SERVICE MANUAL FOR

8500

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TESTING TECHNOLOGY DEPARTMENT / TSSC

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1. Hardware Engineering Specification

1.1 Introduction

The 8500 motherboard would support the Intel® Pentium® 4 processor with FCPGA packaged, mPGA478 Socket, which will supports the different levels up to Willamette P4 1.7GHz (Throttling)/Northwood above 2.0GHz (Throttling).

This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as power indicator, HDD/CDROM, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and Battery charging status. It also equipped 4 USB ports.

The memory subsystem supports 0MB on board memory, two JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM), support PC2100 & PC2700.

SiS650 IGUI Host Memory Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media I/O.

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The SiS961 MuTIOL® Media I/O integrates the Audio Controller with AC 97 Interface, the Ethernet MAC, the Dual Universal Serial Bus Host Controllers, the IDE Master/Slave controllers, and the MuTIOL® Connect to PCI bridge. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O, I/O Advanced Programmable Interrupt Controller and legacy power management functionalities are also integrated. The SiS961 also incorporates an universal interface supporting the asynchronous inputs/outputs of the X86 compatible microprocessors like PIII, K7 and P4.

The SiS301LV/Chrontel CH7017 is a Display Controller device which accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to an LCD panel, while the other data stream is encoded for NTSC or PALTV and outputs through a 10-bit high speed DAC. The TV encoder device encodes a graphics signal up to 1024 x 768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600 x 1200 panels at 60Hz refresh rate.

To provide for the increasing number of multimedia applications, the AC97 CODEC ALC201 is integrated onto the motherboard.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows Me and Windows 2000 to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

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1.2 System Hardware Parts

CPU	Intel Desktop Pentium 4 processor with OLGA Package, uFC-PGA 478 Socket Support up to P4 2.4GHz (Target Thermal ceiling 65W)
Core logic	SiS650+SiS961: Host & Memory & AGP Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance memory controller, a AGP interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media IO.
VGA Control	SiS301LV/Chrontel CH7017
System BIOS	256KB Flash EPROM Inside -Includes System BIOS, VGA BIOS, and plug & Play capability, ACPI
Memory	0MB on board memory -Two JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM) -Support PC2100 & PC2700
Video Memory	8/16/32/64 UMA
Clock Generator **DDR Clock Buffer**	ICS 952001 ICS 93722
IEEE1394	MB86613L
Audio System	AC97 CODEC: Advance Logic, Inc, ALC201 Power Amplifier: TI TPA0202
Super I/O	W83697HG
Modem	56Kbps(V.90, worldwide) MDC Modem
PHY of LAN	ICS1893Y-10 10/100 base T PHY

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1.2.1 CPU_Intel Pentium 4 Processor

The Intel® Pentium® 4 processor, Intel's most advanced, most powerful processor, is based on the new Intel® NetBurst™ micro-architecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multi-media, and multi-tasking user environments. The Intel Pentium 4 processor delivers this world-class performance for consumer enthusiast and business professional desktop users as well as for entry-level workstation users.

Highlights of the Pentium 4 Processor :

- Available at speeds ranging from 1.50 to 2 GHz
- Featuring the new Intel NetBurst micro-architecture
- Supported by the SiS650 chipset
- Fully compatible with existing Intel Architecture-based software
- Internet Streaming SIMD Extensions 2
- Intel® MMX™ media enhancement technology
- Memory cache ability up to 4 GB of addressable memory space and system memory scalability up to 64GB of physical memory
- Support for uni-processor designs
- Based upon Intel's 0.18 micron manufacturing process

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Intel Pentium 4 Processor Product Feature Highlights

The Intel NetBurst micro-architecture delivers a number of new and innovative features including Hyper Pipelined Technology, 400 MHz System Bus, Execution Trace Cache, and Rapid Execution Engine as well as a number of enhanced features Advanced Transfer Cache, Advanced Dynamic Execution, Enhanced Floating-point and Multi-media Unit, and Streaming SIMD Extensions 2. Many of these new innovations and advances were made possible with improvements in processor technology, process technology, and circuit design that could not previously be implemented in high-volume, manufacturable solutions. The features and resulting benefits of the new micro-architecture are defined below.

- Hyper Pipelined Technology:

  The hyper-pipelined technology of the NetBurst micro-architecture doubles the pipeline depth compared to the P6 micro-architecture used on today's Pentium III processors. One of the key pipelines, the branch prediction/ recovery pipeline, is implemented in 20 stages in the NetBurst micro-architecture, compared to 10 stages in the P6 micro-architecture. This technology significantly increases the performance, frequency, and scalability of the processor.

- 400 MHZ System Bus:

  The Pentium4 processor supports Intel's highest performance desktop system bus by delivering 3.2 GB of data per second into and out of the processor. This is accomplished through a physical signaling scheme of quad pumping the data transfers over a 100-MHz clocked system bus and a buffering scheme allowing for sustained 400-MHz data transfers. This compares to 1.06 GB/s delivered on the Pentium III processor's 133-MHz system bus.

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- Level 1 Execution Trace Cache:

  In addition to the 8KB data cache, the Pentium 4 processor includes an Execution Trace Cache that stores up to 12K decoded micro-ops in the order of program execution. This increases performance by removing the decoder from the main execution loop and makes more efficient usage of the cache storage space since instructions that are branched around are not stored. The result is a means to deliver a high volume of instructions to the processor's execution units and a reduction in the overall time required to recover from branches that have been mis-predicted.

- Rapid Execution Engine:

  Two Arithmetic Logic Units (ALUs) on the Pentium 4 processor are clocked at twice the core processor frequency. This allows basic integer instructions such as Add, Subtract, Logical AND, Logical OR, etc. to execute in half a clock cycle. For example, the Rapid Execution Engine on a 1.50 GHz Pentium 4 processor runs at 3 GHz.

- 256KB, Level 2 Advanced Transfer Cache:

  The Level 2 Advanced Transfer Cache (ATC) is 256KB in size and delivers a much higher data throughput channel between the Level 2 cache and the processor core. The Advanced Transfer Cache consists of a 256-bit (32-byte) interface that transfers data on each core clock. As a result, the Pentium 4 processor 1.50 GHz can deliver a data transfer rate of 48 GB/s. This compares to a transfer rate of 16 GB/s on the Pentium III processor at 1 GHz. Features of the ATC include:

  - Non-Blocking, full speed, on-die Level 2 cache
  - 8-way set associativity
  - 256-bit data bus to the level 2 cache
  - Data clocked into and out of the cache every clock cycle

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- Advanced Dynamic Execution:

  The Advanced Dynamic Execution engine is a very deep, out-of-order speculative execution engine that keeps the execution units executing instructions. The Pentium 4 processor can also view 126 instructions in flight and handle up to 48 loads and 24 stores in the pipeline. It also includes an enhanced branch prediction algorithm that has the net effect of reducing the number of branch mis-predictions by about 33% over the P6 generation processor's branch prediction capability. It does this by implementing a 4KB branch target buffer that stores more detail on the history of past branches, as well as by implementing a more advanced branch prediction algorithm.

- Enhanced Floating-Point and Multimedia Unit:

  The Pentium 4 processor expands the floating-point registers to a full 128-bit and adds an additional register for data movement which improves performance on both floating-point and multimedia applications.

- Internet Streaming SIMD Extensions 2 (SSE2):

  With the introduction of SSE2, the NetBurst micro-architecture now extends the SIMD capabilities that MMX technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase. They accelerate a broad range of applications, including video, speech, and image, photo processing, encryption, financial, engineering and scientific applications.

- Features Used for Test and Performance / Thermal Monitoring:
  - Built-in Self Test (BIST) provides single stuck-at fault coverage of the micro-code and large logic arrays, as well as testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs), and ROMs.
  - IEEE 1149.1 Standard Test Access Port and Boundary Scan mechanism enables testing of the Pentium 4 processor and system connections through a standard interface.
  - Internal performance counters can be used for performance monitoring and event counting.
  - Includes a new Thermal Monitor feature that allows motherboards to be cost effectively designed to expected application power usages rather than theoretical maximums.

1.2.2 System Frequency

1.2.2.1 System frequency synthesizer_ICS952001

Programmable Timing Control Hub™ for P4™ processor

General Description :

The ICS952001 is a two chip clock solution for desktop designs using SIS 645/650 style chipsets. When used with a zero delay buffer such as the ICS9179-06 for PC133 or the ICS93705 for DDR applications it provides all the necessary clocks signals for such a system.

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The ICS952001 is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Recommended Application:

SiS645/650 style chipsets

Output features:

- 2 - Pairs of differential CPUCLKs @ 3.3V
- 1 - SDRAM @ 3.3V
- 8 - PCI @3.3V
- 2 - AGP @ 3.3V
- 2 - ZCLKs @ 3.3V
- 1 - 48MHz, @3.3V fixed
- 1 - 24/48MHz, @3.3V selectable by I^2C
- 3 - REF @3.3V, 14.318MHz

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Features/Benefits:

- Programmable output frequency, divider ratios, output rise/fall time, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions
- Programmable watch dog safe frequency.
- Support I^2 C Index read/write and block read/write operations
- For PC133 SDRAM system use the ICS9179-06 as the memory buffer.
- For DDR SDRAM system use the ICS93705 as the memory buffer.
- Uses external 14.318MHz crystal.

Key Specifications:

- PCI - PCI output skew: < 500ps
- CPU - SDRAM output skew: < 1ns
- AGP - AGP output skew: <150ps

1.2.2.2 DDR buffer frequency synthesizer_ICS93722

Low Cost DDR Phase Lock Loop Zero Delay Buffer

Recommended Application:

SiS645/650 style chipsets

Product description/features:

- Low skew, low jitter PLL clock driver
- I^2C for functional and output control
- Feedback pins for input to output synchronization
- Spread Spectrum tolerant inputs
- 3.3V tolerant CLK_INT input

Switching Characteristics

- PEAK - PEAK jitter (66MHz): <120ps
- PEAK - PEAK jitter (>100MHz): <75ps
- CYCLE - CYCLE jitter (66MHz): <120ps
- CYCLE - CYCLE jitter (>100MHz): <65ps
- OUTPUT - OUTPUT skew: <100ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

1.2.3 Core Logic_SiS650 + SiS961

1.2.3.1 SiS650 IGUI Host/Memory Controller

SiS650 IGUI Host Memory Controller integrates a high performance host interface for Intel Pentium 4 processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and SiS MuTIOL® Technology connecting w/ SiS961 MuTIOL® Media IO.

SiS650 Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Pentium 4 processors. SiS650 provides a 12-level In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Pentium 4 series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, SiS650 also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions. A high bandwidth and mature SiS MuTIOL® technology is incorporated to connect SiS650 and SiS961 MuTIOL® Media I/O together. SiS MuTIOL® technology is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in SiS961 to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from SiS650, and the Multi-threaded I/O Link Encoder/Decoder in SiS650 to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from SiS961.

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An Unified Memory Controller supporting PC133 or DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The SiS650 adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

The Integrated GUI features a high performance 3D accelerator with 2 Pixel / 4 Texture, and a 128 bit 2D accelerator with 1T pipeline BITBLT engine. It also features a Video Accelerator and advanced hardware acceleration logic to deliver high quality DVD playback. A Dual 12 bit DDR digital video link interfaced to SiS301B Video Bridge packaged in 100-pin PQFP is incorporated to expand the SiS650 functionality to support the secondary display, in addition to the default primary CRT display. The SiS301B Video Bridge integrates an NTSL/PAL video encoder with Macro Vision Ver. 7.1.L1 option for TV display, a TMDS transmitter with Bi-linear scaling capability for TFT LCD panel support, and an analog RGB port to support a secondary CRT. The primary CRT display and the extended secondary display (TV, TFT LCD Panel, 2'nd CRT) features the Dual View Capability in the sense that both can generate the display in independent resolutions, color depths, and frame rates.

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Two separate buses, Host-t-GUI in the width of 64 bit, and GUI-t-Memory Controller in the width of 128 bit are devised to ensure concurrency of Host-t-GUI streaming, and GUI-t-MC streaming. In PC133, or DDR266 memory subsystem, the 128 bit GUI-t-MC bus will attain the AGP4X or AGP 8X equivalent texture transfer rate, respectively. The Memory Controller mainly comprises the Memory Arbiter, the M-data/M-Command Queues, and the Memory Interface. The Memory Arbiter arbitrates a plenty of memory access requests from the GUI or AGP controller, Host Controller, and I/O bus masters based on a default optimized priority list with the capability of dynamically prioritizing the I/O bus master requests in a bid to offering privileged service to 1) the isochronous downstream transfer to guarantee the min. latency & timely delivery, or 2) the PCI master upstream transfer to curb the latency within the maximum tolerant period of 10us. Prior to the memory access requests pushed into the M-data queue, any command compliant to the paging mechanism is generated and pushed into the M-CMD queue. The M-data/M-CMD Queues further orders and forwards these queuing requests to the Memory Interface in an effort to utilizing the memory bandwidth to its utmost by scheduling the command requests in the background when the data requests streamlines in the foreground.

1.2.3.2 SiS961 MuTIOL® Media I/O overview

The SiS961 MuTIOL® Media I/O integrates the Audio Controller with AC 97 Interface, the Ethernet MAC, the Dual Universal Serial Bus Host Controllers, the IDE Master/Slave controllers, and the MuTIOL® Connect to PCI bridge. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O, I/O Advanced Programmable Interrupt Controller and legacy power management functionalities are also integrated. The SiS961 also incorporates an universal interface supporting the asynchronous inputs/outputs of the X86 compatible microprocessors like PIII, K7 and P4.

The Integrated Audio Controller features a 6 channels of AC 97 v2.2 compliance audio to present 5.1-channel Dolby digital material or to generate stereo audio with simultaneous V.90 HSP modem operation. Besides, 4 separate SDATAIN pins are provided to support multiple audio Codecs + one modem Codec maximally, effectuating the realization of 5.1 channel Dolby digital material in theater quality sound. Both traditional consumer digital audio channel as well as the AC 97 v2.2 compliant consumer digital audio slot are supported. VRA mode is also associated with both the AC 97 audio link and the traditional consumer digital audio channel.

The integrated Fast Ethernet MAC features an IEEE 802.3 and IEEE 802.3x compliant MAC supporting full duplex 10 Base-T, 100 Base-T Ethernet, or 1Mb/s & 10Mb/s Home networking. 5 wake-up Frames, Magic Packet and link status change wake-up functions in G1/G2 states are supported. Besides, the integrated MAC provides a scheme to store the MAC address without the need of an external EEPROM. The 25 MHz oscillating circuit is integrated so as only an external low cost 25 MHz crystal is needed for the clocking system.

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The integrated Universal Serial Bus Host Controllers features Dual Independent OHCI Compliant Host controllers with six USB ports delivering 2 x 12 Mb/s bandwidth and rich connectivity. Besides, each port can be optionally configured as the wake-up source. Legacy USB devices as well as over current detection are also implemented. The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode 0,1,2,3,4, and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment. The MuTIOL® Connect to PCI bridge supporting 6 PCI master is compliant to PCI 2.2 specification. The SiS961 also incorporates the legacy system I/O like: two 8237A compatible DMA controllers, three 8254 compatible programmable 16-bit counters, hardwired keyboard controller and PS2 mouse interface, Real Time clock with 256B CMOS SRAM and two 8259A compatible Interrupt controllers. Besides, the I/O APIC managing up to 24 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the SiS961 supports Intel Speed Step technology and Deeper Sleep power state for Intel Mobile processor. For AMD processor, the SiS961 use the CPUSTP# signal to reduce processor voltage during C3 and S1 state.

1.2.4 SiS301LV/Chrontel CH7017 TV Encoder / LVDS Transmitter

General Description

SiS301LV, which is an accompany chip of SiS VGA chip, integrates :

- A NTSC/PAL video encoder with Macrovision Ver.7.1.L1 option for TV display.
- A LVDS transmitter with bi-linear scaling capability for TFT LCD panel display.

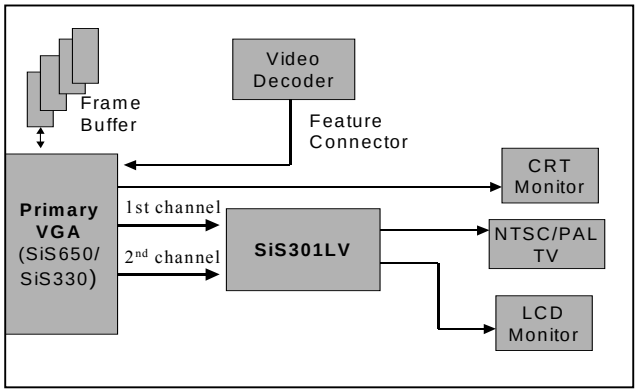
All the above functions can support dual-display features. It means that the second display device driven by SiS301LV can display independent resolutions, color depths and frame rates different from the traditional CRT monitor driven by primary VGA chip. SiS301LV receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S-Video or component video output for TV display, LVDS signals for LCD display. The output display combination can be one of the three :

(1) Primary CRT+SiS301LV TV

(2) Primary CRT+SiS301LV LCD

(3) SiS301LV TV + SiS301LV LCD.

The package type of SiS301LV is 128-pin LQFP.



1.2.4.1 TV Display :

- Supports PAL and NTSC Systems.
- Supports Composite, S-Video, and Component RGB(SCART) Output Signals
- Supports Macrovision Copy Protection Process Rev. 7.1.L1
- Support Progressive TV 525P YPbPr Output Signals.
- Support Macrovision Conpy Protection Waveforms for 525p Progressive Scan Output
- Supports TV/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode
- Provides Adaptive 6-Line Anti-Flicker Filtering.
- Provides Hardware Interpolation for Programmable Under-Scan/Over-Scan Adjustment.
- Provides Programmable Display Position Adjustment.
- Provides Programmable Notch Filter for Cross Color Elimination.
- Provides Chrominance Filter for Cross Luminance Elimination.
- Provides Color Saturation Adjustment for Vivid TV Output.
- Provides Gamma Correction Independent of That of Primary VGA.
- Auto-Sense of TV Connection

1.2.4.2 LVDS Interfaced LCD Panel Display :

- Supports LVDS Transmitter Function.
- Single LVDS supports pixel rate up to 110M pixel/sec.
- Compatible with TIA/EIA-644 LVDS standard.
- Provides Bi-linear Scaling to Scale VGA Low Resolution Mode up for LCD Display – up to 1280x1024
- Supports LCD/Primary VGA Independent Display Resolution and Frame Rate at Enhanced Mode.
- Support 2D dither for 18-bit panels.
- Provides Programmable Display Centering.
- Compliant with VESA DDC2B
- Compliant with VESA Plug & Display, Hot Plugging Function.

1.2.5 AC'97 Audio System: Advance Logic, Inc, ALC201

SiS961 is an AC'97 2.1 compliant controller that communicates with companion Codecs SiS a digital serial link called the AC-link.

The ALC201 is an AC97 2.2 compatible stereo audio codec designed for PC multimedia systems.The ALC201 provides the way for PC98 and PC99-compliant desktop, portable and entertainment PCs, where high-quality audio is required. The ALC201 AC'97 CODEC provides a complete high quality audio solution.

Features

- Single chip audio CODEC with high S/N ratio (>90 dB)
- 18-bit ADC and DAC resolution
- Compliant with AC'97 2.2 specification
- Meet performance requirements for audio on PC2001 systems
- 18-bit stereo full-duplex CODEC with independent and variable sampling rate
- 4 analog line-level stereo input with 5-bit volume control: LINE_IN, CD, VIDEO, AUX
- 2 analog line-level mono input: PC_BEEP, PHONE_IN
- Mono output with 5-bit volume control
- Stereo output with 5-bit volume control
- 2 MIC inputs: Software selectable
- Power management

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- 3D Stereo Enhancement
- Headphone output with 50mW/20ohm driving capability (ALC201)
- Line output with 50mW/20ohm driving capability (ALC201A)
- Headphone jack-detect function to mute LINE output
- Multiple CODEC extension
- MC'97 chained in allowed for multi-channel application
- External Amplifier power down capability
- Support S/PDIF out is fully compliant with AC'97 specification rev2.2
- DC offset cancellation
- Power support: Digital: 3.3V An*alog: 5V*
- Standard 48-Pin LQFP Package

1.2.6 MDC: PCTel Modem Daughter Card PCT2303W

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1.

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The chip set is fully programmable to meet worldwide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

Operating System Compatibility

- Windows 98 /NT4.0 /Win 2K /Win XP

Compatibility

ITU-T V.90	56000, 54667, 53333,52000, 50667, 49333, 48000, 46667, 45333, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000bps
K56Flex	56000, 54000, 52000, 50000, 48000, 46000, 44000, 42000, 40000, 38000, 36000, 32000bps
ITU-T V.34Annex	33600,31200 bps
ITU-T V.34	28800 bps
ITU-T V.32bis	14400 bps
ITU-T V.32	9600,4800 bps
ITU-T V.22bis	2400 bps
ITU-T V.22	1200 bps
ITU-T V.21	300 bps
ITU-T V.23	1200/75 bps

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- ITU-T V.17 14400,12000,9600,7200 bps
- ITU-T V.29 9600,7200 bps
- ITU-T V.27ter 4800,2400 bps
- Bell 212A 1200 bps
- Bell 103 300 bps

Modulation

- 56000bps (V90&K56Flex) PCM
- 33600 bps (V.34Annex) TCM
- 28800 bps (V.34) TCM
- 14400 bps (V.32bis) TCM
- 12000 bps (V.32bis) TCM
- 9600 bps (V.32bis) TCM
- 7200 bps (V.32bis) QAM
- 9600 bps (V.32) TCM, QAM
- 4800 bps (V.32) QAM
- 14400 bps (V.17) TCM
- 12000 bps (V.17) TCM
- 9600 bps (V.29) QAM
- 7200 bps (V.29) QAM
- 4800 bps (V.27ter) DPSK

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- 2400 bps (V.27ter) DPS
- 2400 bps (V.22bis) QAM
- 1200/75bps (V.23) FSK
- 1200bps (V.22/Bell 212A) DPSK
- 300bps (V.21/Bell 103) FSK

Data Compression

- V.42bis, MNP5

Error Correction

- V.42 LAPM, MNP 2-4

DTE interface

DTMF Tone Frequency

Low Group Frequency (Hz)

		697	770	852	941
High Group	1209	1	4	7	*
Frequency	1336	2	5	8	0
(Hz)	1477	3	6	9	#
	1633	A	B	C	D

DTMF signal level

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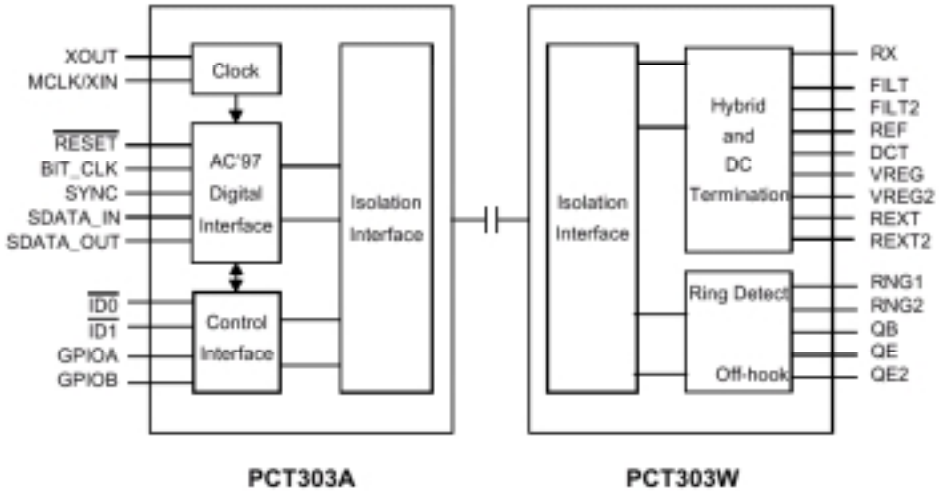
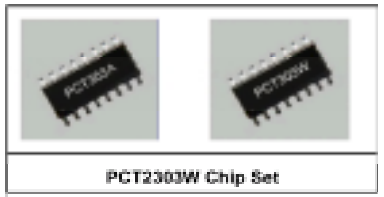
1.2.6.1 High Group -10+/-2dBm

1.2.6.2 Low Group -12+/-2dBm

- Dialing Type — Tone or pulse dialing
- Telephone Line interface — RJ-11
- Return Loss — 300HZ - 3400HZ >= 10db
- Flow Control — XOFF/XON or RTS/CTS
- Receive Level — -35 +/- 2dBm
- Transmit Level — >-15 dBm

Specification and features subject to change without notice!





1.2.7 IEEE1394 Open HCI Controller

Overview

MB86613S is Fujitsu's IEEE1394- OHCI (Open Host Controller Interface) Controller LSI that is compliant with IEEE1394- 1995, P1394a and OHCI (revision 1.1, release) standard drafts. This LSI integrates both 1394 PHY and LINK layers including analog PLL, transceiver, and comparator circuits using Fujitsu's advanced full CMOS process for the cost- effective single- chip solution.

In addition to the 1394 block, the MB86613S contains various DMA engines called ContextProgram Controllers used for OHCI functions and PCI block. ContextProgram block consists of total 13 channels of independent DMA that are each dedicated to asynchronous and isochronous transmit and isochronous – asynchronous common receive operations. On- chip, 5V and 3.3V operable, PCI bus controller is compliant with PCI local bus standard (revision2.2) incorporating one 32- bit DMA controller and power management functions as specified in PCI bus power management specification (version 1.1).

For valuable host side design, this chip also incorporates serial Configuration ROM interface.

The device operates by +5V or +3.3V power supply for the PCI andDMA blocks and +3.3V for the whole 1394 block.

To provide with the cost- effective solution, the LSI is housed in a 100- pin plastic small QFP package.

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Features

1394 Serial Bus Controller Block:

- Compliant with IEEE1394- 1995 and P1394a draft2.0
- Integrates PHY and LINK layers into single- chip.
- 1394 port number : 1 port
- Transfer Data Rate : S100, S200, and S400
- On- chip PLL : 400MHz for PHY and 50MHz for Link core.
- Cycle- Master Function
- On- chip Bus Management CSRs
- 6- pin cable supported
- On- chip transceiver and comparator
- On- chip another comparator for detecting the cable power

ContextProgram Controller Block :

- Compliant with Open HCI standard draft (revision 1.1)
- Total 13 independent ContextProgram Controllers:
  - Asynchronous Transmit DMA : 2 channels for response and request each
  - Isochronous Transmit DMA : 4 channels
  - Receive DMA : 7 channels for Asynchronous response and request each, 4 isochronous, and 1 self- ID receive

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Preliminary :

- On- chip 6KB FIFO :
  - Asynchronous T ransmit- FIFO : 1.5KB
  - Isochronous Transmit- FIFO : 1.5KB
  - Asynchronous/Isochronous Receive- FIFO : 3.0KB
- On- chip context program work memory : 128B x 3

PCI Bus Controller Block :

- Compliant with PCI local bus specification (revision 2.2)
- On- chip 32- bit DMA controller
- On- chip power management (PCI power management standard, revision 1.1, compliant)
- Alignment function
- Byte swap function
- 33MHz operation
- On- chip serial ROM interface
- On- chip universal type (5V/3.3V) PCI buffer

Others :

- 100- pin plastic LQFP package
- Two power supply systems : +5V and +3.3V

1.2.8 Keyboard System: HT82K68E

General Description

The HT82K68E is an 8-bit high performance peripheral interface IC, designed for multiple I/O products and multimedia applications. It supports interface to a low speed PC with multimedia keyboard or wireless keyboard in Windows 95, Windows 98 or Windows 2000 environment. A HALT feature is included to reduce power consumption.

Features

- Operating voltage: 2.4V~5.5V
- 32/34 bidirectional I/O lines
- One 8-bit programmable timer counter with overflow interrupts
- Crystal or RC oscillator
- Watchdog Timer
- 3K_16 program EPROM
- 160_8 data RAM
- One external interrupt pin (shared with PC2)
- HALT function and wake-up feature reduce power consumption
- Six-level subroutine nesting
- Bit manipulation instructions

- 16-bit table read instructions
- 63 powerful instructions
- All instructions in 1 or 2 machine cycles
- 20/28-pin SOP, 40-pin DIP, 48-pin SSOP package

1.2.9 System Flash Memory (BIOS)

- 2 M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program

1.2.10 Memory System

64MB, 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SO-DIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 64MB (8 Meg x 64 [H]); 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 2.5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge

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- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bi-directional data strobe (DQS) transmitted/received with data—i.e.,source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4 or 8
- Auto precharge option
- KBC and PS2 mouse can be individually disabled
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

1.2.11 PHY: 3.3-V 10Base-T/100Base-TX Integrated PHYceiver The ICS1893 is a low-power, physical-layer device (PHY)

General Description

The ICS1893 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TXCarrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards. The ICS1893 architecture is based on the ICS1892. The ICS1893 supports managed or unmanaged node, repeater, and switch applications.

The ICS1893 incorporates digital signal processing (DSP) in its Physical Medium Dependent (PMD) sublayer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100 MHz. With this ICS-patented technology, the ICS1893 can virtually eliminate errors from killer packets.

The ICS1893 provides a Serial Management Interface for exchanging command and status information with a Station Management (STA) entity.

The ICS1893 Media Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 MHz or 100 MHz. The MDI configuration can be established manually (with input pins or control register settings) or automatically (using the Auto-Negotiation features). When the ICS1893 Auto-Negotiation sublayer is enabled, it exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode they have in common.

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Features

- Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz across a temperature range from –5 to +85 C
- DSP-based baseline wander correction to virtually eliminate killer packets across temperature range from -5 to +85 C
- Low-power, 0.35-micron CMOS (typically 400 mW)
- Single 3.3-V power supply
- Single-chip, fully integrated PHY provides PCS, PMA, PMD and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - NLT-3 encoder and NRZ/NRZI encoder
- Highly configurable design supports:
  - Node, repeater, and switch applications
  - Managed and unmanaged applications
  - 10M or 100M half- and full-duplex modes
  - Parallel detection
  - Auto-negotiation, with Next Page capabilities
- MAC/Repeater Interface can be configured as:
  - 10M or 100M Media Independent Interface
  - 100M Symbol Interface (bypasses the PCS)
  - 10M 7-wire Serial Interface
- Small Footprint 64-pin Thin Quad Flat Pack (TQFP)

1.3 Other Functions

1.3.1 Hot Key Functions

Keys Combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power on/off/suspend/resume button

APM mode

At APM mode, Power button is on/off system power.

ACPI mode

At ACPI mode. Windows power management control panel set power button behavior.
You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.
Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.
At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.3.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

- AC Power: This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.
- Battery Power: This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.

1.3.5 Fan power on/off management

FAN is controlled by H8 embedded controller-using AD2201 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.6 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.
- Battery was put in battery holder, can be replaced.

1.3.7 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- Supports two USB port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- Headphone Out Jack.
- Microphone Input Jack.
- Line in Jack

1.3.8 Battery current limit and learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.4 Peripheral Components

	VIA Solution	SiS Solution
CPU	- Intel D/T Pentium 4 Processors Willamette/Northwood with OLGA Package, mPGA478 Socket - Support up to P4 Willamette 2.0GHz / Northwood 2.4GHz - FSB 400MHz	
Core Logic	VIA P4N266 + VT8233	SiS650 + SiS961
Memory	DDR SO-DIMM module 128/256MB support PC2100 Specification - ATP : AT16L64A8S4B0S (128MB) / AT16L64A8S4A2S (128MB) - Apacer : 77.1032.460 (128MB), 77.10521.460 (128MB), 77.10621.110 (256MB)	
CD-ROM	- TEAC : CD-224E-B92 - MKE : CR-177-B - QSI : SCR242	
DVD-ROM	- QSI : SDR-081 - MKE : SR-8176-B - TEAC : DV2-28E-B93	
Combo Drive	- KME : UJDA710MT - QSI : SBW-081	
CD-RW	- MKE : UJDA-330 - QSI : SCW-081	
External USB FDD	Mitsumi : D353G (3.5” 1.44MB/1.2MB/720KB FDD)	
HDD	- IBM: 10GB : IC25N010ATDA040-0, 20GB : IC25N020ATDA040-0, 30GB : IC25N010ATDA040-0 - Hitachi : 10GB : DK23CA-10, 15GB : DK23CA-15, 20GB : DK23CA-20, 30GB : DK23CA-30 - Fujitsu : 10GB : MHN2100AT, 15GB : MHN2115AT, 20GB : MHN2200AT, 30GB : MHN2230AT	
Display	- 14” TFT XGA : 1. Hyundai : HT14X13-102 2. Chi-mei : N141X201 3. QDI : QD141X1LH03 - 15” TFT XGA : 1. Samsung : LT150X3-124 2. Hannstar : HS150PX11-B - 15” TFT SXGA+ : 1. Samsung : LTN150P1-L03	

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Video Controller	Integrated in VIA P4N266	Integrated in SiS650
Pointing Device	Synaptics : TM41PD350	
Audio	- Audio Power Amplifier : TI - AC 97 Codec : VIA : VT1611A	- Audio Power Amplifier : TI - AC 97 Codec : ALC201
PCMCIA	- ENE : CB1410 - TI : PCI1410	
Keyboard	JME 19mm pitch/3.0mm stroke	

1.5 Power Management

The 8500 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

Full on mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability. The CPU power consumption and temperature is lower in this mode.

Standby mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

- CPU: Stop grant
- LCD: backlight off
- HDD: spin down

Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- Suspend to DRAM:
  - CPU: off
  - Twister K: Partial off
  - VGA: Suspend
  - PCMCIA: Suspend
  - Audio: off
  - SDRAM: self refresh
- Suspend to HDD:
  - All devices are stopped clock and power-down
  - System status is saved in HDD
  - All system status will be restored when powered on again

1.5.2 Other Power Management Functions

HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 Appendix 1: SiS961 GPIO Definitions

SB_SiS961 GPIO

Signal Name	MUX Function	Mitac Definition	Buffer Type	Power Plane	Tolerant	During PCISRT#	After PCISRT#	S1	S3	S4/S5
GPIO0		MB_ID0	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO1	LDRQ1#	CD_IN#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO2	THERM#	SB_THRM#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO3	EXTSMI#	EXTSMI#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO4	CLKRUN#	CLKRUN#	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO5	PREQ5#	LCD_ID0	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO6	PGNT5#	LCD_ID1	I/O	Main		Driven Defined	Driven Defined	Driven Defined	Off	Off
GPIO7		LCD_ID2	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO8	RING#	WAKEUP#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO9	AC_SDIN2	SCI#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO10	AC_SDIN3	CRT_IN#	I/O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO11		SPK_OFF	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO12	CPUSTP#	CPU_STP#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO13	DPRSLPVR	MPCIACT# /DPRSLPVR	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO14		CD_PWRON#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO15	VR_HILO#	VR_HILO#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO16	LO_HI#	LO_HI#	OD	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO17	VGATEM#	VGATEM#	I/O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO18	PMCLK	CD_RST	O	AUX		Driven Defined	Driven Defined	Driven Defined	Driven Defined	Driven Defined
GPIO19	SMBCLK	SMBCLK	O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z
GPIO20	SMBDATA	SMBDATA	O	AUX		High-Z	High-Z	High-Z	High-Z	High-Z

1.7 Appendix 2: 8500 Product Specifications

CPU	Intel Desktop Pentium 4 Processors with OLGA Package, uFC-PGA478 Socket Support up to P4 2.4GHz (Target Thermal ceiling 65W)
Chipset	**SiS650 + SiS961**
L2 Cache	256KB
System BIOS	Flash EPROM (Include System BIOS and VGA BIOS)
Memory	0MB on board; 200-pin DDR-RAM Memory Module x 2
ROM Drive	12.7mm Height 24X CD ROM Drive 8X DVD ROM Drive 8X4x24 CD-RW or above 8X8X4X24 Combo or above
HDD	2.5x9.5 mm height: 10/15/20/30GB; Support Ultra DMA 66/100 Reseller Exchangeable
FDD	Support FDD 3.5" Format for 720KB/1.2MB/1.44MB
Display	14.1"/ 15" XGA TFT display; Resolution: 1024 x 768
Video Controller	Integrated in SiS650 Chipset Support Multi Monitor Support AGP 4X
Keyboard	19mm pitch/3.0mm stroke Windows Logo Key x 1; Application Key x 1
Pointing Device	Glide pad with 2x buttons and 1x scroll button
Card Reader	CF + SM + SD Card

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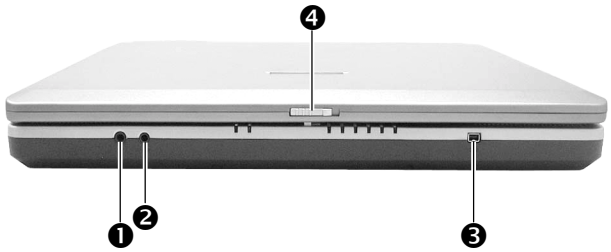
Audio System	Sound Blaster Pro compatible Support AC97 2.1	Built-in mono microphone 2X Speakers (1Watt each)
I/O Port	Bi-directional Parallel Port (EPP/ECP) x 1 RJ-11 port x 1 DC input x 1 Audio-out x 1 (SPIDF) TV-Out x 1 LCD Cover Switch x 1	Standard USB1.1 port x 2 RJ-45 port x 1 VGA monitor port x1 Mic-in x 1 Microphone x 1
Communication	Built-in 56Kbps V.90 MDC modem Built-in 10/100 based-T LAN	
Wireless Commuication	Reserved for Mini-PCI Wireless LAN (IEEE 802.11b standard) (Factory Option)	
Power Supply	External battery 12-cell li-ion (2000mAH/3.7V) with charge circuit (Charge by AC ADPT)	
AC adapter	Universal AC adapter 90W ; Input: 100-240V, 50/60Hz AC	
Dimensions	330 x 278 x 42mm (Max)	
Weight	3.5Kg	
Accessories	Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title	
Manual Printings	EN, GR, CH, Pan-EU	
Agency	FCC, CE, UL, TUV, CB, BSMI	
Architecture	Support PC2001 Specification, Designed for Windows ME, Windows 2000 & Windows XP	
Options	64/128/256MB DDRAM, AC Adapter w/o Power Cord, Notebook Carry Bag	

2. System View and Disassembly

2.1 System View

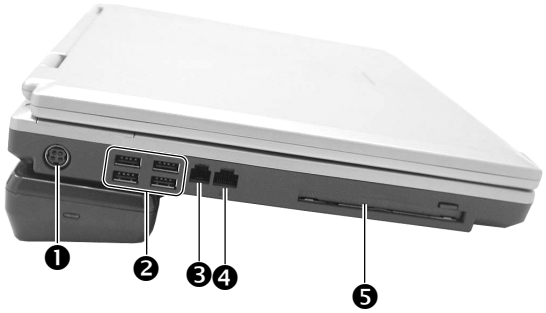
2.1.1 Front View

❶ External Microphone Jack
❷ Line Out Phone Jack
❸ Mini IEEE1394 Connector
❹ Top Cover Latch



2.1.2 Left-side View

❶ Power Jack
❷ USB Ports
❸ RJ-11 Connector
❹ RJ-45 Connector
❺ PC Card Slot

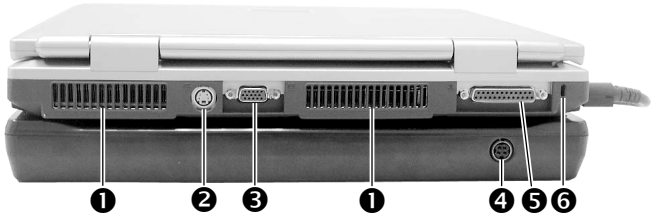


2.1.3 Right-side View

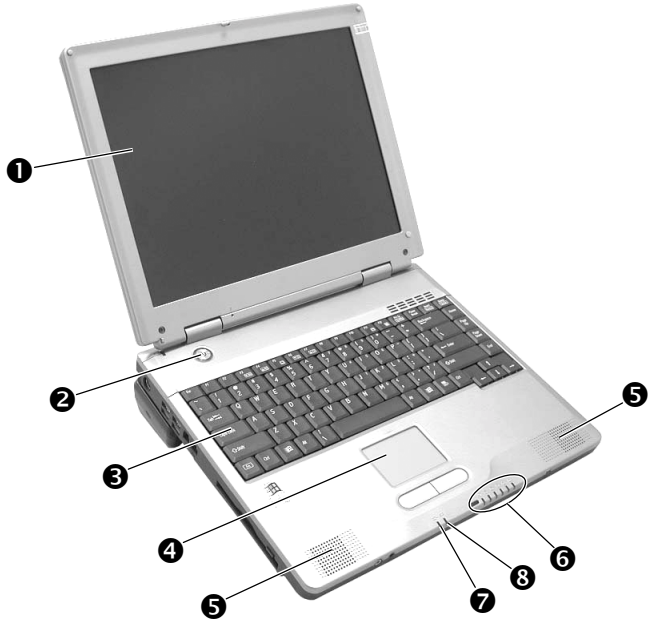
❶ CD-ROM/DVD-ROM Drive

2.1.4 Rear View

❶ Ventilation Openings
❷ S-Video Output Connector
❸ VGA Port
❹ Power Jack
❺ Parallel Port
❻ Kensington Lock



2.1.5 Top-open View

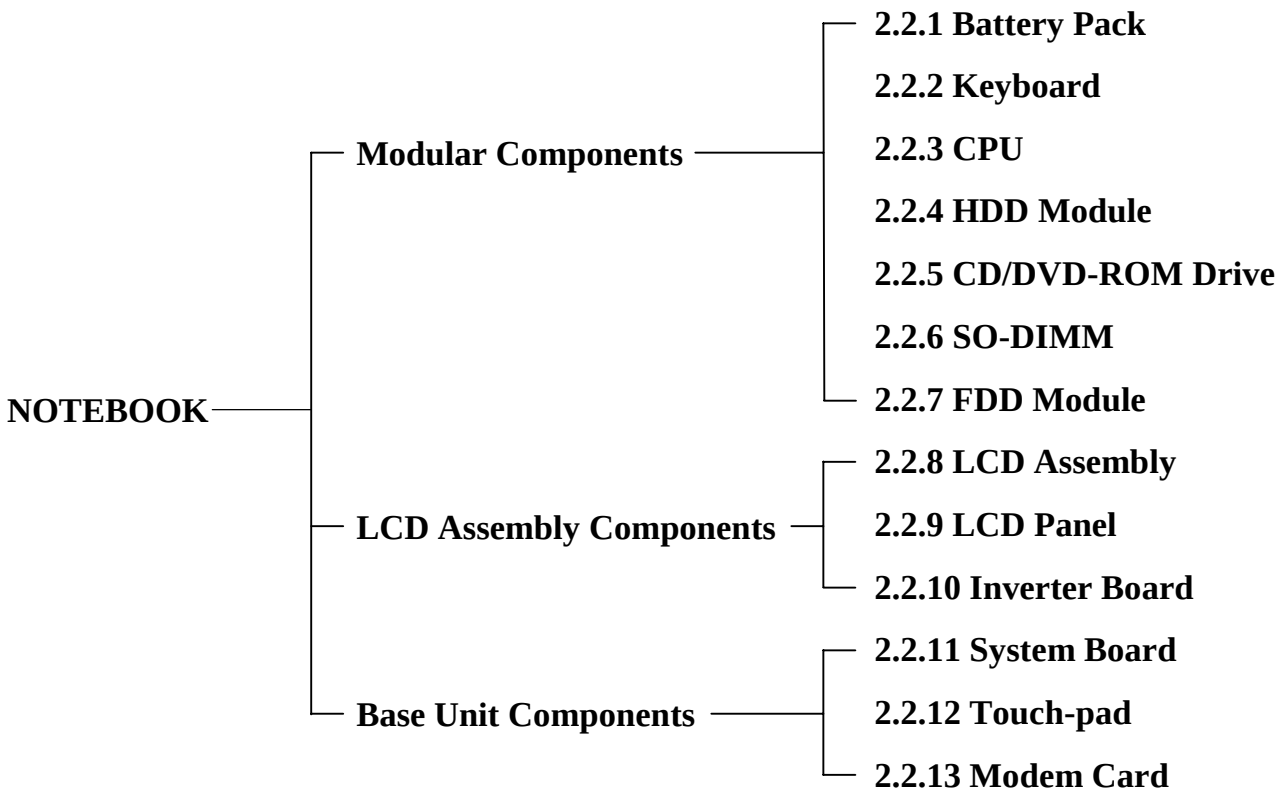


❶ LCD Screen
❷ Power Button
❸ Keyboard
❹ Touch Pad
❺ Stereo Speaker Set
❻ Device Indicator
❼ Power Indicator
❽ Battery Charge Indicator

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Disconnect the battery power cable. (Figure 2-1)

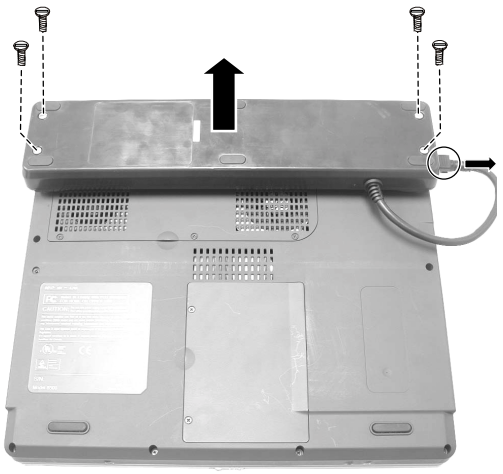


Figure 2-1 Remove the battery pack

3. Loosen four screws fastening the Battery pack, then lift it up. (Figure 2-1)

Reassembly

1. Replace the battery pack and secure with four screws.
2. Reconnect the battery power cable.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Carefully put the notebook upside down. And remove one screw locking the KB cover. (Figure 2-2)

Figure 2-2 Remove the screw

Figure 2-3 Remove KB cover

3. Open the top cover. Push and slide the KB cover to the right (❶). Then lift the KB cover up (❷). (Figure 2-3)

4. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-4)

Figure 2-4 Disconnect the keyboard cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Slide the KB cover toward left and ensure it was well.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Remove three screws fastening the heatsink cover. (Figure 2-5)

Figure 2-5 Remove the cover

Figure 2-6 Remove the heatsink

3. Remove three screws fastening the heatsink and disconnect the two fan's power cords from system board. (Figure 2-6)

4. Loosen the screw by a flat screwdriver, upraise the CPU socket to unlock the CPU. (See Figure 2-7)

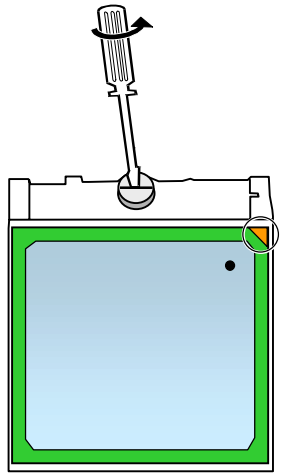


Figure 2-7 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Fasten the CPU by a flat screwdriver.
2. Reconnect the two fan's power cords to the system board, fit the heatsink onto the top of the CPU and secure with three screws.
3. Replace the heatsink cover and secure with three screws.
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 disassembly)
3. Remove the two screws fastening the HDD compartment cover. (Figure 2-8)

Figure 2-8 Remove HDD cover

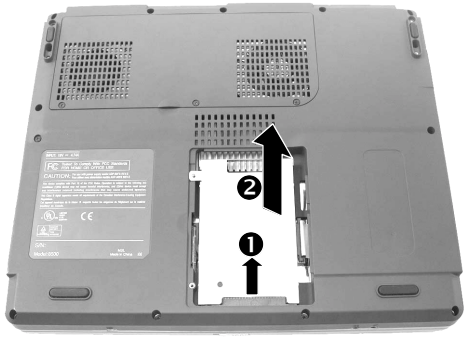


Figure 2-9 Remove the HDD module

4. Slide the hard disk drive outward to unplug the connector (❶)and take out the hard disk drive (❷). (Figure 2-9)

5. Remove the four screws on the both side of hard disk drive bracket, then lift drive up. (Figure 2-10)

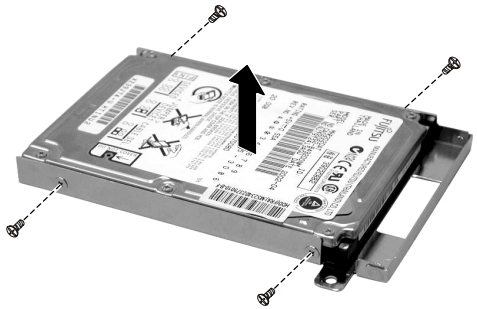


Figure 2-10 Remove hard disk drive

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with four screws.
2. Slide the HDD module into the compartment to plug.
3. Replace the HDD compartment cover.
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 disassembly)
3. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-11)
4. Put the notebook back to the upright position. Then insert a small rod, such as a straightened paper clip, into the drive's manual eject hole and push firmly to release the tray (❶). Pull the tray out until fully extended, then carefully pull harder to remove the CD/DVD-ROM drive (❷). (Figure 2-11)

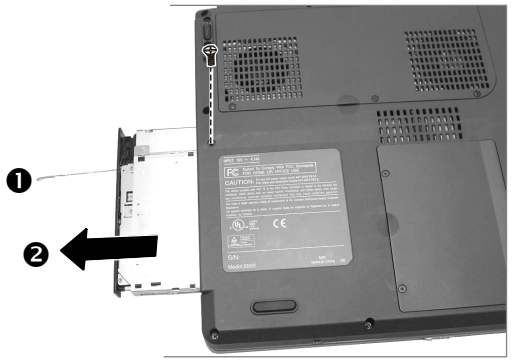


Figure 2-11 Remove the CD/DVD-ROM drive

Reassembly

1. To replace the CD/DVD-ROM drive, slide and push it all the way into the compartment to plug.
2. Secure the CD/DVD-ROM drive with one screw.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.6 SO-DIMM

Disassembly

1. Remove the battery pack and the keyboard. (See section 2.2.1 and 2.2.2 disassembly)
2. Full the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-12)

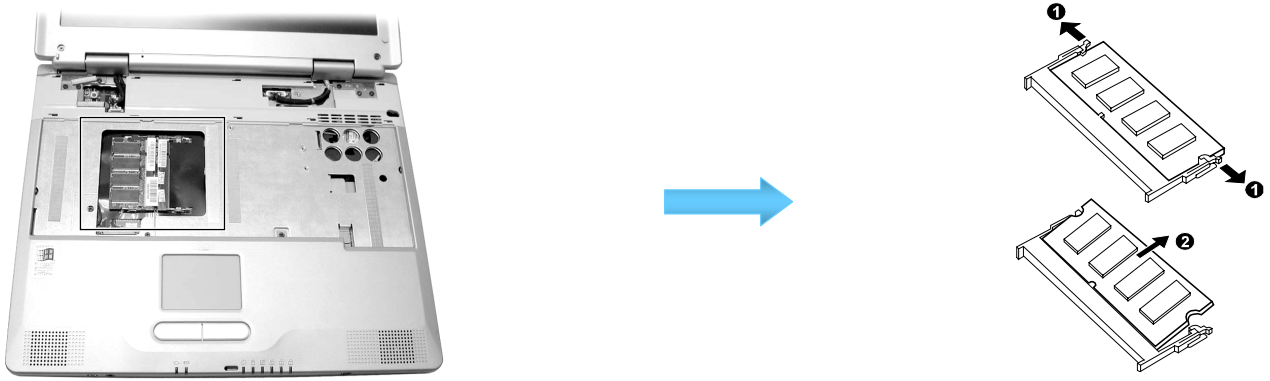


Figure 2-12 Remove the SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the OS-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into cover.
2. Fit the keyboard and the battery pack. (See section 2.2.1 and 2.2.2 reassembly)

2.2.7 FDD Module

Disassembly

1. Remove the battery pack, keyboard, HDD module and the CD/DVD-ROM. (See section 2.2.1, 2.2.2, 2.2.4, 2.2.5 Disassembly)
2. Remove the two screws fastening the housing. (Figure 2-13)

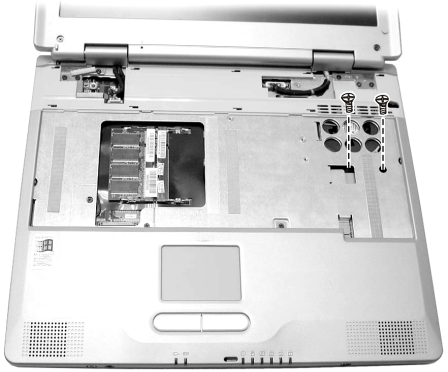


Figure 2-13 Remove two screws

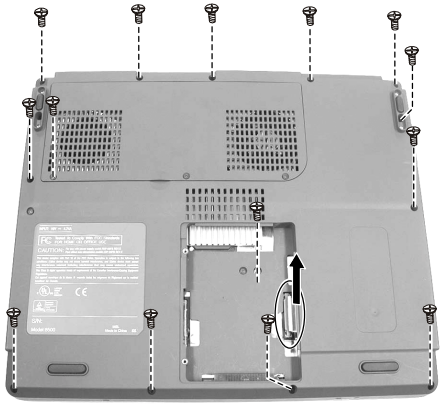


Figure 2-14 Remove the housing

3. Put it upside down . Remove fourteen screws on the bottom of the notebook and disconnect one cable. Then separate the housing with FDD module. (Figure 2-14)

4. Remove two screws fastening the FDD module. Now you can detach the FDD module from housing. (Figure 2-15)

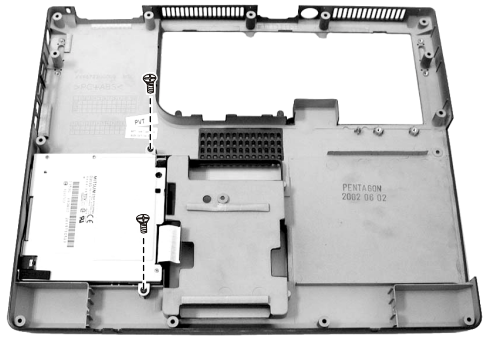


Figure 2-15 Remove two screws

Reassembly

1. Fit the FDD module back into place and secure with two screw.
2. Fit the housing and secure with fourteen screws. Then connect the cable.
3. Turn over the notebook and fasten the housing by the two screws.
4. Replace the CD/DVD-ROM, HDD module, Keyboard and the battery pack. (See section 2.2.5, 2.2.4, 2.2.2, 2.2.1 disassembly)

2.2.8 LCD Assembly

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Open the LCD assembly. Remove the keyboard . (See section 2.2.2 Disassembly)
3. Remove the two hinge covers and disconnect the LCD cables from the system board. (Figure 2-16)
3. Remove six screws fastening the LCD assembly. Now you can separate the LCD assembly from the base unit. (Figure 2-16)

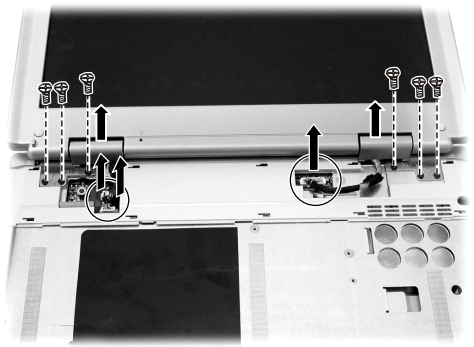


Figure 2-16 Remove the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with six screws on the hinges.
2. Reconnect the LCD cables to the system board. And replace two hinge cover.
3. Fit the keyboard . (See section 2.2.2 reassembly)
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.9 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.8 Disassembly)
2. Remove the two rubber pads and two screws on the lower part of the panel. (figure 2-17)
3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.

Figure 2-17 Remove LCD frame

Figure 2-18 Remove LCD panel

4. Remove the four screws on two sides and four screws on the lower part of the LCD panel, and disconnect the cable from the inverter board. (Figure 2-18)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the two screws and two rubber pads.
3. Replace the LCD assembly. (See section 2.2.8 reassembly)

2.2.10 Inverter Board

Disassembly

1. Remove the LCD assembly. (See section 2.2.8 Disassembly)
2. To remove the inverter board on the bottom side of the LCD assembly, disconnect the cable and remove two screw. (Figure 2-19)

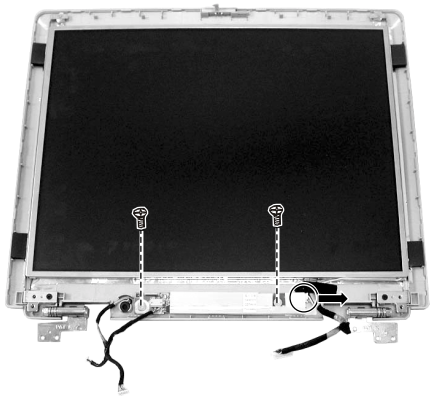


Figure 2-19 Remove the inverter board

Reassembly

1. Fit the inverter board back into place and secure with two screw. And reconnect the cable to inverter board.
2. Replace the LCD assembly. (See section 2.2.8 Reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See section 2.2.1 to 2.2.5 and 2.2.8 Disassembly)
2. Remove two screws fastening the top cover and remove two screws fastening the housing. (Figure 2-20)

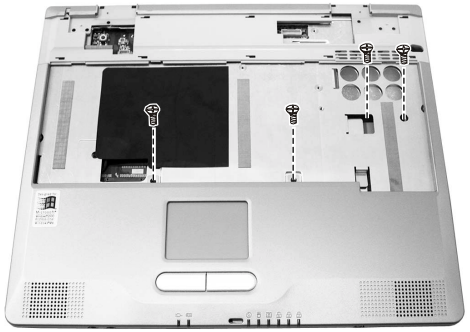


Figure 2-20 Remove four screws

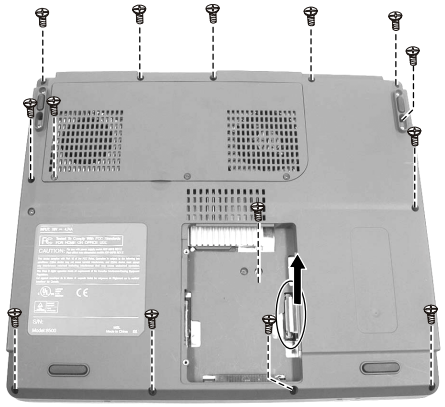


Figure 2-21 Remove the housing

3. Put it upside down. Remove fourteen screws on the bottom of the notebook and disconnect one cable. Then separate the housing. (Figure 2-21)

4. Disconnect the touch pad cable, two speaker set's cords and remove four screws fastening the system board. Then lift the system board up. (Figure 2-22)

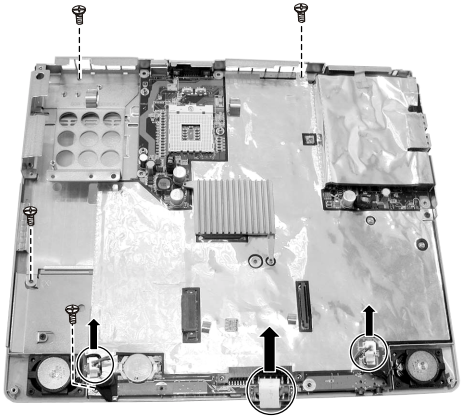


Figure 2-22 Remove the system board ASSY

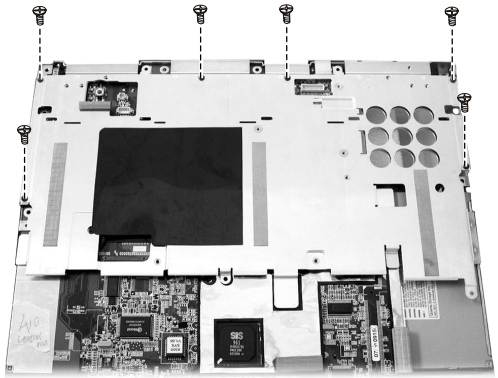


Figure 2-23 Remove the plate shield

5. Remove the six screws fastening the plate shield. (Figure 2-23)

6. Remove four hex nuts fastening the system board on the rear side of the system board and one screw on the top of the system board. Carefully separate the system board from IO bracket. (Figure 2-24)

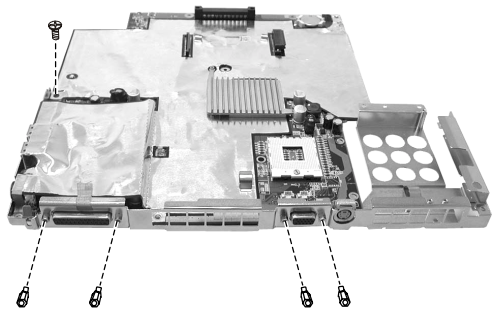


Figure 2-24 Remove the system board

Reassembly

1. Fit the system board into IO bracket and secure with four hex nuts and one screw.
2. Replace the plate shield and secure with six screws.
3. Fit the system board back into the top cover, then reconnect touch pad's cable and the two speaker set's cords to system board and secure with four screws.
4. Fit the housing and secure with fourteen screws.
5. Fit the top cover and secure with four screws.
6. Replace the LCD assembly, CD/DVD-ROM drive, HDD module, CPU, keyboard and battery pack. (See section 2.2.8, 2.2.5 to 2.2.1 reassembly)

2.2.12 Touch pad

Disassembly

1. Remove the battery pack, keyboard, heatsink, HDD module, CD/DVD-ROM drive and LCD assembly. (See section 2.2.1,2.2.2 and 2.2.8 disassembly)
2. To separate the top cover, remove the system board ASSY. (See steps 2—4 of the section 2.2.11 disassembly)
3. Remove the seven screws fastening the touch pad shield. (Figure 2-25)

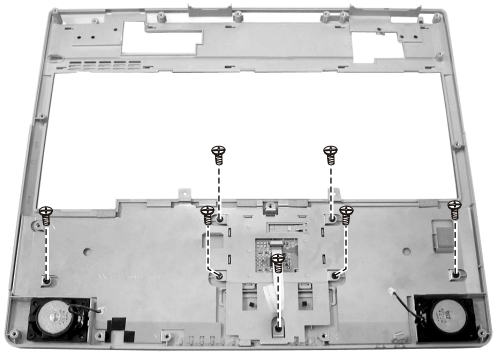


Figure 2-25 Remove the touch-pad

Reassembly

1. Fit the touch pad and secure, then replace the shield on the touch pad and secure with seven screws.
2. Assemble the notebook. (See steps 2—6 of the section 2.2.11 Reassemble)

2.2.13 Modem Card

Disassembly

1. Remove the battery pack, keyboard, heatsink, HDD module, CD/DVD-ROM drive, and LCD assembly. (See section 2.2.1 to 2.2.5 and 2.2.8 Disassembly)
2. Disassemble the notebook to access the system board. (See steps 1—5 of the section 2.2.11 Disassembly)
3. Remove the two screws fastening the modem card, and then disconnect the cable from system board. (Figure 2-26)

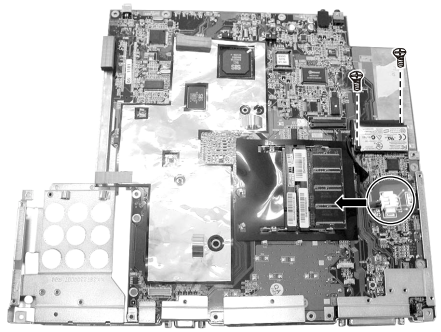


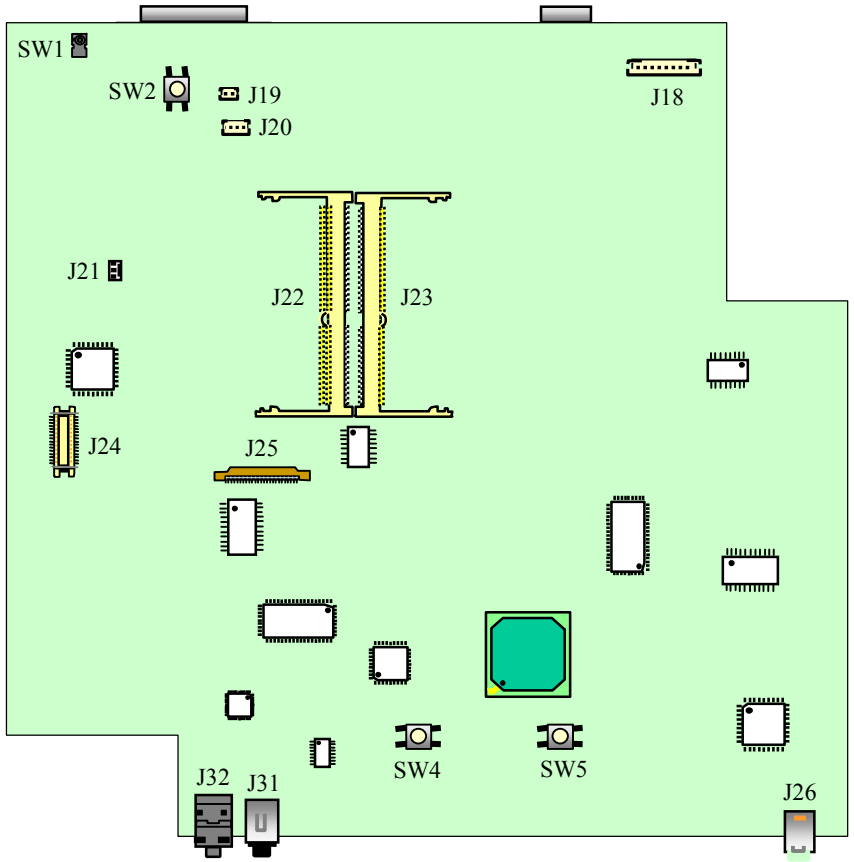
Figure 2-26 Remove the Modem card

Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See steps 2—4 of the section 2.2.11 Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board – A



- **J18 : LCD Connector**
- **J19 : Internal Microphone Connector**
- **J20 : Inverter Board Connector**
- **J21 : MDC Jump Wire Connector**
- **J22 : 200-pin expansion DDR SDRAM Socket**
- **J23 : 200-pin expansion DDR SDRAM Socket**
- **J24 : MDC Connector**
- **J25 : Internal Keyboard Connector**
- **J26 : IEEE 1394 Port**
- **J31 : Line Out Phone Jack**
- **J32 : External Microphone Jack**
- **SW1 : Cover Switch**
- **SW2 : Power Switch**
- **SW4 : Touch-pad Left Button**
- **SW5 : Touch-pad Right Button**

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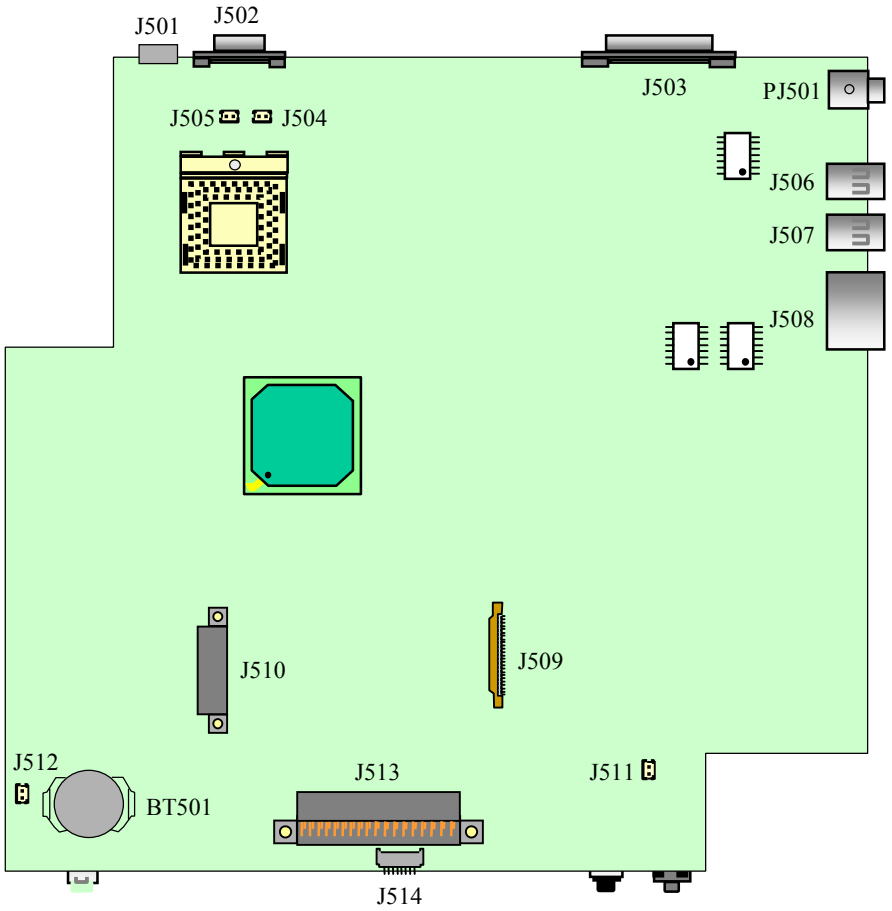
3. Definition & Location of Connectors / Switches

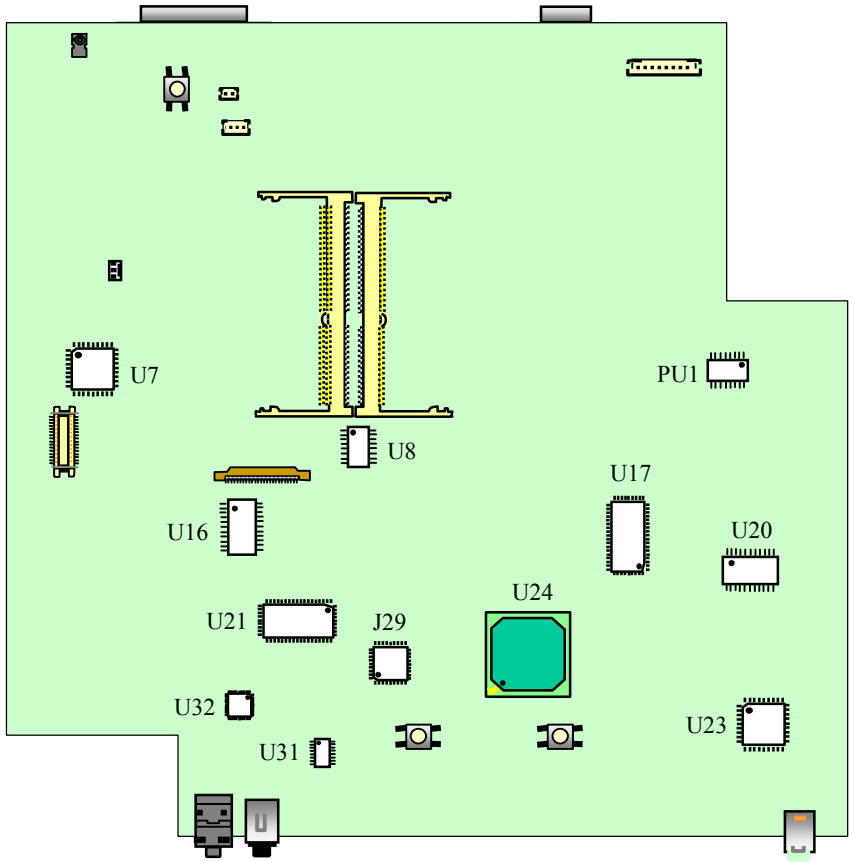
3.1 Mother Board – B



- **J501 : TV Out Jack**
- **J502 : External VGA Connector**
- **J503 : Parallel Port Connector**
- **J504 : FAN Connector**
- **J505 : FAN Connector**
- **J506 : USB Port Connector**
- **J507 : USB Port Connector**
- **J508 : Modem (RJ11)/LAN (RJ45) Connector**
- **J509 : Floppy Connector**
- **J510 : Secondary IDE Connector**
- **J511 : L-Speaker Connector**
- **J512 : R-Speaker Connector**
- **J513 : Primary IDE Connector**
- **J514 : Touch-pad Connector**
- **PJ501 : Power Jack**
- **BT501 : CMOS Battery**

4. Definition & Location of Major Components

4.1 Mother Board - A



- U7 : ISC1893Y LAN Controller
- U8 : ICS93722 Clock Buffer
- U16 : Internal Keyboard Encoder
- U17 : SiS301LV/Chrontel CH7017
- U20 : ICS952001 Clock Generator
- U21 : W83697HF Super I/O Controller
- U23 : MB86613L IEEE 1394 Controller
- U24 : SiS961 MuTIOL Media I/O Controller
- U31 : LM4873LQ Audio Amplifier
- U32 : ALC202 Audio Codec
- PU1 : MAX1632 +3V/+5V/+12V Generator
- J29 : System BIOS

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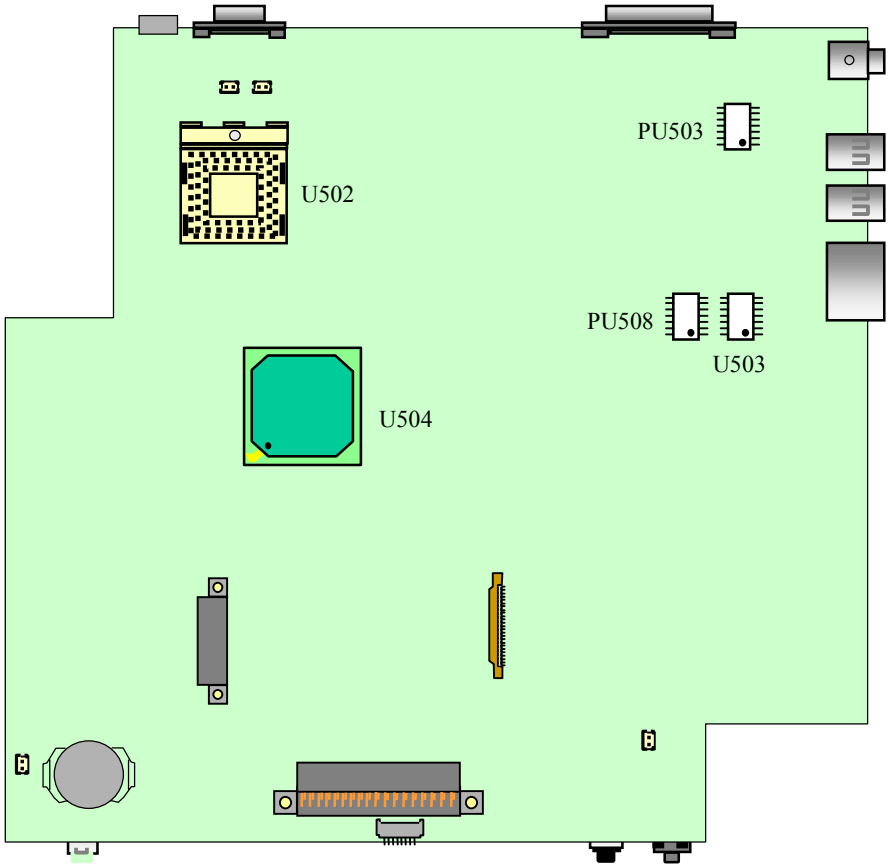
4. Definition & Location of Major Components

4.1 Mother Board - B



- **U502 : Intel NorthWood P4 Processor**
- **U503 : PH163112 LAN Buffer**
- **U504 : SiS650 IGUI Host/Memory Controller**
- **PU503 : HIP6301 VCC_CORE Generator**
- **PU508 : MAX1714A +2.5V_DDR Generator**

5. Pin Descriptions of Major Components

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2 36 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** **REQ[4:0]#, A[16:3]#** / **ADSTB0#** **A[35:17]#** / **ADSTB1#**
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines **Request Signals** / **subphase 1** / **subphase 2** **A[35:24]#** / **AP0#** / **AP1#** **A[23:3]#** / **AP1#** / **AP0#** **REQ[4:0]#** / **AP1#** / **AP0#**
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V CROSS .
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for termination requirements.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
BSEL[1:0]	Output	The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Pentium 4 processor in the 478-pin package operates currently at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency).
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for details on implementation.

Name	Type	Description
D[63:0]#	Input/ Output	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#. **Quad-Pumped Signal Groups** **Data Group / DSTBN#/ DSTBP# / DBI#** **D[15:0]# — 0 — 0** **D[31:16]# — 1 — 1** **D[47:32]# — 2 — 2** **D[63:48]# — 3 — 3** Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	Input/ Output	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DBI[3:0] Assignment To Data Bus** **Bus Signal / Data Bus Signals** **DBI3# — D[63:48]#** **DBI2# — D[47:32]#** **DBI1# — D[31:16]#** **DBI0# — D[15:0]#**
DBR#	Output	DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.

5.1 Intel Pentium 4 Processor mPGA478 Socket

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
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<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr>
</table></td></tr>
<tr><td>FERR#</td><td>Output</td><td>FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.</td></tr>
<tr><td>GTLREF</td><td>Input</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 Vcc. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide for more information.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>HIT#

HITM#</td><td>Input/ Output

Input/ Output</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>IERR#</td><td>Output</td><td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
This signals does not have on-die termination.</td></tr>
<tr><td>IGNNE#</td><td>Input</td><td>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>INIT#</td><td>Input</td><td>INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).</td></tr>
<tr><td>ITPCLKOUT[1:0]</td><td>Output</td><td>The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package.</td></tr>
<tr><td>ITP_CLK[1:0]</td><td>Input</td><td>ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.</td></tr>
</table>

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. .

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Intel Pentium 4 Processor mPGA478 Socket

Name	Type	Description
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow he guidelines for VCCA, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
VCCSENSE	Output	VCCSENSE is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSSSENSE	Output	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 SiS650 IGUI Host/Memory Controller

Host BUS Interface

Name	Pin Attr	Signal Description
CPUCLK **CPUCLK#**	I 0.71V – M	**Host differential clock input.**
CPURST#	O 1.2~1.85V – M O	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
CPUPWRGD#	1.2~1.85V – M	**CPUPWRGD#** is used to inform CPU that main power is stable
ADS#	I/O 1.2~1.85V – M	**Address Strobe :** Address Strobe is driven by CPU or SiS650 to indicate the start of a CPU bus cycle.
HADSTB[1:0]#	1.2~1.85V – M	**Source synchronous address strobe** used to latch HREQ[4:0]# & HA[31:3]# at both falling and rising edge. HREQ[4:0]# & HA[16:3]# are latched by HASTB0# HA[31:17] are latched by HASTB1#
HREQ[4:0]#	I/O 1.2~1.85V – M	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
HA[31:3]#	I/O 1.2~1.85V – M	**Host Address Bus**
BREQ0#	O 1.2~1.85V – M	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BPRI#	O 1.2~1.85V – M	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
BNR#	I/O 1.2~1.85V – M	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	I 1.2~1.85V – M	**Host Lock** : CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	I/O 1.2~1.85V – M	**Keeping a Non-Modified Cache Line**
HITM#	I/O 1.2~1.85V – M	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1/L2 cache of CPU.
DEFER#	O 1.2~1.85V – M	**Defer Transaction Completion:** r defer response to host bus.

Host BUS Interface Continue

Name	Pin Attr	Signal Description
RS[2:0]#	O 1.2~1.85V – M	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. RS[2:0] Response 000 Idle State 001 Retry 010 Defer 011 Reserved 100 Reserved 101 No data 110 Implicit Write-back 111 Normal Data
HTRDY#	O 1.2~1.85V – M	**Target Ready:** During write cycles, response agent will drive TRDY# to indicate it is ready to accept data.
DRDY#	I/O 1.2~1.85V – M	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O 1.2~1.85V – M	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
HD[63:0]#	I/O 1.2~1.85V – M	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
DBI[3:0]#	I/O 1.2~1.85V – M	**Dynamic Bus Inversion:** An active DBI# will invert **it**'s corresponding data group signals. DBI0# is referenced by HD[15:0], DBI1# is referenced by HD[31:16] DBI2# is referenced by HD[47:32] DBI3# is referenced by HD[63:48]
HDSTBP[3:0]#	I/O 1.2~1.85V – M	**Source synchronous data strobe** used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBP0# HD[31:16], DBI1# are latched by HDSTBP1# HD[47:32], DBI2# are latched by HDSTBP2# HD[63:48], DBI3# are latched by HDSTBP3#
HDSTBN[3:0]#	I/O 1.2~1.85V– M	**Source synchronous data strobe** used to latch data at falling edge HD[15:0], DBI0# are latched by HDSTBN0# HD[31:16], DBI1# are latched by HDSTBN1# HD[47:32], DBI2# are latched by HDSTBN2# HD[63:48], DBI3# are latched by HDSTBN3#
HNCOMP	I M	**GTL N-MOS Compensation Input**

5.2 SiS650 IGUI Host/Memory Controller

Host BUS Interface Continue

Name	Pin Attr	Signal Description
HPCOMP	I M	**GTL P-MOS Compensation Input**
HVREF[4:0] **HNCOMPVREF**	I M	**AGTL+ I/O reference voltage**

DRAM Controller

Name	Pin Attr	Signal Description
SDCLK	I 3.3V - M	**SDRAM Clock Input**
SDRCLKI	I 2.5V/3.3V - M	**SDRAM Read Clock Input**
FWDSDCLKO	O 2.5V/3.3V – M	**SDRAM Forward Clock Output**
MA[14:0]	O 2.5V/3.3V - M	**System Memory Address Bus**
SRAS#	O 2.5V/3.3V - M	**SDRAM Row Address Strobe**
SCAS#	O 2.5V/3.3V - M	**SDRAM Column Address Strobe**
SWE#	O 2.5V/3.3V - M	**SDRAM Write Enable**
CS[5:0]# **CSB[5:0]#**	O 2.5V/3.3V - M	**SDRAM Chip Select** **CSB[5:0] multiplexed with DQS[5:0]**
DQM[7:0]#	O 2.5V/3.3V - M	**SDRAM Input/Output Data Mask**
DQS[7:0]	I/O 2.5V/3.3V - M	**DDR Data Strobe**
MD[63:0]	I/O 2.5V/3.3V - M	**System Memory Data Bus**
CKE[5:0]	O (open-drain) 2.5V/3.3V – AUX	**SDRAM Clock Enable**
S3AUXSW# **(CKE6)**	O (open-drain) 2.5V/3.3V - AUX	**Aux power switch for ACPI-S3 state, low active.**
DDRVREF[A:B]	I M	**DDR I/O Reference Voltage**

SiS MuTIOL Interface

Name	Pin Attr	Signal Description
ZCLK	I 3.3V - M	**SiS MuTIOL Connect**
ZUREQ/ZD **REQ**	I/O 1.8V - M	**SiS MuTIOL Connect Control pins**
ZSTB[1:0]	I/O 1.8V - M	**SiS MuTIOL Connect Strobe**
ZSTB[1:0]#	I/O 1.8V - M	**Strobe Compliment**
ZAD[15:0]	I/O 1.8V - M	**I/O** **1.8V - M**
ZVREF	I M	**SiS MuTIOL Connect Reference Voltage**
ZCMP_N	I M	**N-MOS Compensation Input**
ZCMP_P	I M	**P-MOS Compensation Input**

SiS MuTIOL Interface Continue

Name	Pin Attr	Signal Description
AGPCLK	I 3.3V – M	**AGP Clock**
AFRAME#	I/O 1.5V/3.3V - M	**AGP Frame#**
AIRDY#	I/O 1.5V/3.3V - M	**AGP Initiator Ready**
ATRDY#	I/O 1.5V/3.3V - M	**AGP Target Ready**
ASTOP#	I/O 1.5V/3.3V - M	**AGP Stop#**
ADEVSEL#	I/O 1.5V/3.3V - M	**AGP Device Select**
ASERR#	I 1.5V/3.3V - M	**AGP System Error**
AREQ#	I 1.5V/3.3V - M	**AGP Bus Request**
AGNT#	O 1.5V/3.3V - M	**AGP Bus Grant**
AAD[31:0]	I/O 1.5V/3.3V - M	**AGP Address/Data Bus**

5.2 SiS650 IGUI Host/Memory Controller

SiS MuTIOL Interface

Name	Pin Attr	Signal Description
AC/BE[3:0]	I/O 1.5V/3.3V - M	**AGP Command/Byte Enable**
APAR	I/O 1.5V/3.3V - M	**AGP Parity**
ST[2:0]	O 1.5V/3.3V - M	**AGP Status Bus**
PIPE#	I 1.5V/3.3V - M	**AGP Pipeline Request**
SBA[7:0]	I/O 1.5V/3.3V - M	**Side Band Address**
RBF#	I 1.5V/3.3V - M	**Read Buffer Full**
WBF#	I 1.5V/3.3V - M	**Write Buffer Full**
AD_STB[1:0]	I/O 1.5V/3.3V - M	**AD Bus Strobe**
AD_STB[1:0]#	I/O 1.5V/3.3V - M	**AD Bus Strobe Compliment**
SB_STB	I 1.5V/3.3V - M	**Side Band Strobe**
SB_STB#	I 1.5V/3.3V - M	**Side Band Strobe Compliment**

Stereo Glasses Interface

Name	Pin Attr	Signal Description
CSYNC	O 3.3V - M	**Stereo Clock**
RSYNC	O 3.3V - M	**Stereo Right**
LSYNC	O 3.3V - M	**Stereo Left**

VB Interface

Name	Pin Attr	Signal Description
VBCLK	I 1.8V/3.3V - M	**Channel B/A Clock Input** VBCLK multiplexed with SBA0
VBHCLK	O 1.8V/3.3V – M	**VB Programming Interface Clock** VBHCLK multiplexed with RBF#
VBCAD	I/O 1.8V/3.3V – M	**VB Programming Interface Data** VBCAD multiplexed with AREQ#
VBCTL[1:0]	O 1.8V/3.3V - M	**VB Data Control** VBCTL[1:0] multiplexed with AAD[29:28]
VGPIO[3:2]	I/O 3.3V - M	**VB GPIO pins** VGPIO[3:2] multiplexed with PIPE#/WBF#
VBHSYNC	I/O 1.8V/3.3V - M	**Channel B H-Sync** VBHSYNC multiplexed with AAD30
VBVSYNC	I/O 1.8V/3.3V - M	**Channel B V-Sync** VBVSYNC multiplexed with AAD31
VBDE	I/O 1.8V/3.3V - M	**Channel B Data Valid** VBDE multiplexed with AAD27
VBGCLK	I/O 1.8V/3.3V - M	**Channel B Clock Output.** This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VBGCLK multiplexed with AD_STB1
VBD[11:0]	I/O 1.8V/3.3V - M	**Channel B Data** VBD[11:0] multiplexed with AAD
VAHSYNC	I/O 1.8V/3.3V - M	**Channel A H-Sync** VAHSYNC multiplexed with AAD18
VAVSYNC	I/O 1.8V/3.3V - M	**Channel A V-Sync** VAVSYNC multiplexed with AAD17
VADE	I/O 1.8V/3.3V - M	**Channel A Data Valid** VADE multiplexed with AAD16
VAGCLK	I/O 1.8V/3.3V - M	**Channel A Clock Output.** This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VAGCLK multiplexed with AD_STB0
VAGCLK#	I/O 1.8V/3.3V - M	**Channel A Differential Clock Output. (**To support Chrontel). VAGCLK# multiplexed with AD_STB0#
VAD[11:0]	I/O 1.8V/3.3V - M	**Channel A Data** VAD[11:0] multiplexed with AAD

5.2 SiS650 IGUI Host/Memory Controller

VGA Interface

Name	Pin Attr	Signal Description
VOSCI	I 3.3V - M	**14.318 Reference Clock Input**
HSYNC	O 3.3V - M	**Horizontal Sync**
VSYNC	O 3.3V - M	**Vertical Sync**
INTA#	O 3.3V - M	**Internal VGA Interrupt Pin**
VGPIO[1:0]	I/O 3.3V - M	**Internal VGA GPIO pins**
VCOMP	AI Analog - M	**Compensation Pin**
VRSET	AI Analog - M	**Reference Resistor**
VVBWN	AI Analog - M	**Voltage Reference**
ROUT	AO Analog - M	**Red Signal Output**
GOUT	AO Analog - M	**Green Signal Output**
BOUT	AO Analog - M	**Blue Signal Output**

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attribute
A1XAVDD	3.3V	MAIN	Analog
A1XAVSS	0V	GROUND	Analog
A4XAVDD	3.3V	MAIN	Analog
A4XAVSS	0V	GROUND	Analog
AGPVSSREF	0V	GROUND	Analog
AUX1.8	1.8V	AUX	Digital
AUX3.3	3.3V	AUX	Digital
C1XAVDD	3.3V	MAIN	Analog
C1XAVSS	0V	GROUND	Analog

Power and Ground Signals continue

Name	Tolerance	Power Plane	Type Attribute
C4XAVDD	3.3V	MAIN	Analog
C4XAVSS	0V	GROUND	Analog
DACAVDD1	1.8V	MAIN	Analog
DACAVDD2	1.8V	MAIN	Analog
DACAVSS1	0V	GROUND	Analog
DACAVSS2	0V	GROUND	Digital
DCLKAVDD	3.3V	MAIN	Digital
DCLKAVSS	0V	GROUND	Analog
DDRAVDD	3.3V	MAIN	Analog
DDRAVSS	0V	GROUND	Analog
ECLKAVDD	3.3	MAIN	Analog
ECLKAVSS	0V	GROUND	Analog
IVDD	1.8V	MAIN	Digital
OVDD	3.3V	MAIN	Digital
PVDD	3.3V	MAIN	Digital
PVDDM	3.3V	AUX	Digital
PVDDP	1.8V	MAIN	Digital
PVDDZ	1.8V	MAIN	Digital
SDAVDD	3.3V	MAIN	Analog
SDAVSS	0V	GROUND	Analog
VDDM	2.5/3.3V	MAIN(AUX)	Digital
VDDQ	1.5/1.8/3.3V	MAIN	Digitalv
VDDZ	1.8V	MAIN	Digital
VDDMCMP	1.8V	MAIN	Analog
VTT	1.2~1.85V	MAIN	Digital
Z1XAVDD	3.3V	MAIN	Analog
Z1XAVSS	0V	GROUND	Analog
Z4XAVDD	3.3V	MAIN	Analog
Z4XAVSS	0V	GROUND	Analog

5.2 SiS650 IGUI Host/Memory Controller

Test Mode/Hardware Trap/Power Management

Name	Pin Attr	Signal Description
DLLEN#	I/O 3.3V/5V - M	**Hardware Trap pin (refer to section 5)**
DRAM_SEL	I 3.3V/5V - AUX	**Hardware Trap pin (refer to section 5)**
TRAP[1:0]	I 3.3V/5V - M	**Hardware Trap pins (refer to section 5)**
ENTEST	I 3.3V/5V - M	**Test Mode enable pin**
TESTMODE[2:0]	I 3.3V/5V - M	**Test Mode select pin** **Nand Tree Test: 100**
AUXOK	I 3.3V - AUXI	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PCIRST#	I 3.3V - AUXI	**PCI Bus Reset :** PCIRST# is supplied from SiS MuTIOL Media IO SiS961.
PWROK	I 3.3V - AUXI	**Main Power OK :** A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

5.3 SiS961 MuTIOL Media I/O Controller

Host Bus Interface

Name	Pin Attr	Signal Description
FERR#	I 1.1V/2.65V -M	**Floating Point Error:** CPU will assert this signal upon a floating point error occurring.
IGNNE#	OD 1.1V/2.65V -M	**Ignore Numeric Error:** IGNNE# is asserted to inform CPU to ignore a numeric error.
NMI	OD 1.1V/2.65V -M	**Non-Maskable Interrupt:** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	OD 1.1V/2.65V -M	**Interrupt Request:** High-level voltage of this signal conveys to CPU that there is outstanding interrupt(s) needed to be serviced.
APICD[1:0]	I/OD 1.1V/2.65V -M	**APIC Data:** These two signals are used to send and receive APIC data.
CPUSLP#/ CPUSTP#	OD 1.1V/2.65V -M	**CPU Sleep:** The CPUSLP# can be used to force CPU enter the Sleep state. **CPU Clock STOP:** For Intel Mobile processor, this signal can be used to stop the clock to the processor. If the processor is in Quick Start state and the processor clock is stopped, the processor will enter the Deep Sleep state. For AMD processor, this signal can be to reduce processor voltage during C3/S1 state.
STPCLK#	OD 1.1V/2.65V -M	**Stop Clock:** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs
INIT#	OD 1.1V/2.65V -M	**Initialization:** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium III platform it is active high. This signal requires an external pull-up resistor tied to 3.3V.
APICCK	I 2.5V - M	**APIC Clock:** This signal is used to determine when valid data is being sent over the APCI bus.
A20M#	OD 1.1V/2.65V- M	**Address 20 Mask:** When A20M# is asserted, the CPU A20 signal will be forced to “0”

MuTIOL Connect Interface

Name	Pin Attr	Signal Description
ZCLK	I 3.3V - M	**Megaband I/O Connect Clock**
ZUREQ	I/O 1.8V - M	**Megaband I/O Conect Controll pins**
ZDREQ	I/O 1.8V - M	**Megaband I/O Conect Controll pins**
ZSTB[1:0]	I/O 1.8V - M	**Megaband I/O Connect Strobe**
ZSTB[1:0]#	I/O 1.8V - M	**Strobe Compliment**
ZAD[15:0]	I/O 1.8V - M	**Address/Data pins**
ZVRE	I -M	**Megaband I/O Connect I/O reference voltage**
ZCMP_N	I -M	**N-MOS Compensation Input**
ZCMP_P	I -M	**P-MOS Compensation input**

PCI Interface Continue

Name	Pin Attr	Signal Description
PCICLK	I 3.3V/5V -M	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS961. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O 3.3V/5V -M	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS961 is a PCI bus master and inputs when it is a PCI slave.
PLOCK#	I/O 3.3V/5V -M	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS961 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.

5.3 SiS961 MuTIOL Media I/O Controller

PCI Interface Continue

Name	Pin Attr	Signal Description
AD[31:0]	I/O 3.3V/5V -M	**PCI Address /Data Bus:** In address phase: 1.When the SiS961 is a PCI bus master, AD[31:0] are output signals. 2.When the SiS961 is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS961 is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS961 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O 3.3V/5V -M	**Parity:** SiS961 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	I/O 3.3V/5V -M	**Frame#:** FRAME# is an output when the SiS961 is a PCI bus master. The SiS961 drives FRAME# to indicate the beginning and duration of an access. When the SiS961 is a PCI slave device, FRAME# is an input signal.
IRDY#	I/O 3.3V/5V -M	**Initiator Ready:** IRDY# is an output when the SiS961 is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS961 is a PCI slave, IRDY# is an input pin.
TRDY#	I/O 3.3V/5V -M	**Target Ready:** TRDY# is an output when the SiS961 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS961 is a PCI master, it is an input pin.
STOP#	I/O 3.3V/5V -M	**Stop#:** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.

PCI Interface

Name	Pin Attr	Signal Description
DEVSEL#	I/O 3.3V/5V -M	**Device Select:** As a PCI target, SiS961 asserts DEVSEL# by doing positive or subtractive decoding. SiS961 positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS961 is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PREQ[4:0]#	I 3.3V/5V -M	**PCI Bus Request:** PCI Bus Master Request Signals
PGNT[4:0]#	O 3.3V –M	**PCI Bus Grant:** PCI Bus Master Grant Signals
PREQ5# / **GPIO5**	I I/O 3.3V/5V- M	**PCI Bus Request:** PCI Bus Master Request Signal
PGNT5# / **GPIO6**	O I/O 3.3V- M	**PCI Bus Grant:** PCI Bus Master Grant Signal
INT[A:D]#	I 3.3V/5V –M	**PCI interrupt A,B,C,D:** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	O 3.3V –M	**PCI Bus Reset:** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	I 3.3V/5V –M	**System Error:** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

5.3 SiS961 MuTIOL Media I/O Controller

IED Interface

Name	Pin Attr	Signal Description
IDA[15:0]	I/O 3.3V/5V -M	Primary Channel Data Bus
IDB[15:0]	I/O 3.3V/5V -M	Secondary Channel Data Bus
IDECSA[1:0]#	O 3.3V -M	Primary Channel CS[1:0]
IDECSB[1:0]#	O 3.3V -M	Secondary Channel CS[1:0]
IIOR[A:B]#	O 3.3V -M	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	O 3.3V -M	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	I 3.3V/5V -M	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	O 3.3V -M	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	O 3.3V -M	Primary Channel Address [2:0]
IDSAB[2:0]	O 3.3V -M	Secondary Channel Address [2:0]
CBLID[A:B]	I 3.3V/5V -M	Primary/Secondary Ultra-66 Cable ID

Legacy I/O and Miscellaneous Signals

Signal Name	Pin Attr	Signal Description
SPK	O 3.3V -M	**Speaker output:** The SPK is connected to the system speaker.
ENTEST	I 3.3V/5V -M	SiS961 Test Mode Enable Pin
OSCI	I 3.3V -M	SiS961 Test Mode Enable Pin

Power Management Interface

Name	Pin Attr	Signal Description
ACPILED	OD <=5V -AUX	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1Hz to indicate the system is at power saving mode.
EXTSMI# / GPIO3	I I/O 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
PME#	I 3.3V/5V -AUX	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#.
PSON#	OD <=5V -AUX	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
AUXOK	I 3.3V -AUX	**Auxiliary Power OK:** This signal is supplied from the AUX power source. It is also used to reset the logic in AUX power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PWRBTN#	I 3.3V/5V -AUX	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
RING / GPIO8	I I/O 3.3V/5V -AUX	**Ring Indication:** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
BCLK_STP# GPIO12	O I/O 3.3V/5V -AUX	**Stop CPU clock:** Output to the external clock generator for it to turn off the CPU clock during C3/Sx.
DPRSLPVR GPIO13	O O 3.3V/5V -AUX	**Deeper Sleep:** DPRSLP# can be used to lower the Intel processor voltage during C3/S1 state.

5.3 SiS961 MuTIOL Media I/O Controller

LPC Interface

Name	Pin Attr	Signal Description
LAD[3:0]	I/O 3.3V/5V-M	**LPC Address/Data Bus:** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	I 3.3V/5V-M	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LDRQ1# / GPIO1	I I/O 3.3V/5V-M	**LPC DMA Request 1:** This pin is used by LPC device to request DMA cycle.
LFRAME#	O 3.3V -M	**LPC Frame:** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	I/O 3.3V/5V -M	I/O 3.3V/5V -M

TRC Interface

Name	Pin Attr	Signal Description
BATOK	I 3.3V -RTC	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	I 3.3V-RTC	**RTC 32.768 KHz Input:** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	O <3.3V -RTC	**RTC 32.768 KHz Output:** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an external oscillator is used.
PWROK	I 3.3V-RTC	**Main Power OK**: A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, PCIRST# will all be asserted until after PWROK goes high for 12 ms.

AC'97 Interface

Name	Pin Attr	Signal Description
AC_BIT_CLK	I 3.3V/5V -M	**AC'97 Bit Clock:** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	O 3.3V -AUX	**AC'97 Reset:** Hardware reset signal for external Codecs.
AC_SDIN0	I 3.3V/5V -AUX	**AC'97 Serial Data Input :** Serial data input from primary Codec.
AC_SDIN1	I 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from secondary Codec. When Modem Codec is used, this pin dedicate to Modem Serial data input.
AC_SDIN[3:2]/ GPIO[10:9]	I I/O 3.3V/5V -AUX	**AC'97 Serial Data Input:** Serial data input from third and forth Audio Codec.
AC_SDOUT	O 3.3V -M	**AC'97 Serial Data Output:** Serial data output to Codecs.
AC_SYNC	O 3.3V -M	**AC'97 Synchronization:** This is a 48KHz signal, which is used to synchronize the Codecs

USB Interface

Name	Pin Attr	Signal Description
USBCLK48M	I 3.3V/5V -M	**USB 48 MHz clock input:** This signal provides the fundamental clock for the USB Controller.
OC[0:5]#	I/O 3.3V/5V - AUX	**USB Port 0-5 Overcurrent Detection:** OC[0:5]# are used to detect the overcurrent condition of USB Ports 0-5.
UV[2:0]+, UV[2:0]-	I/O 3.3V - AUX	**USB Port** [**2:0**] **Differential**: These differential pairs are used to transmit Data/Address /Command signals for ports 0-2. (USB controller 1)
UV[5:3]+, UV[5:3]-	I/O 3.3V - AUX	**USB Port [5:3] Differential**: These differential pairs are used to transmit Data/Address/ Command signals for ports 3-5. (USB controller 2)

5.3 SiS961 MuTIOL Media I/O Controller

Keyboard Control Interface

Name	Pin Attr	Signal Description
KBDAT / GPIO15	I/OD O/OD 3.3V/5V -AUX	**Keyboard Dada:** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK / GPIO16	I/OD O/OD 3.3V/5V -AUX	**Keyboard Clock:** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT / GPIO17	I/OD O/OD 3.3V/5V -AUX	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal.
PMCLK / GPIO18	I/OD O/OD 3.3V/5V -AUX	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal.

MAC Interface Continue

Name	Pin Attr	Signal Description
RXER	I 3.3V/5V -AUX	**RX Packet Error** This event is signaled after the last received descriptor in a failed packet reception that has been updated with valid status.
MIICLK25M	I 3.3V/5V -AUX	**PHY 25MHz Clock Input:** This pin provides the 25MHz clock signal input to the built-in oscillator.
MDC	O 3.3V -AUX	**Management Data Clock:** Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external physical unit on the MIIMDIO pin.
TXD[0:3]	I 3.3V/5V -AUX	**Receive Data:** This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXCLK by the external physical unit.
TXEN	O 3.3V -AUX	**Transmit Data:** This is a group of 4 data signals which are driven synchronous to the TXCLK for transmission to the external physical unit.
RXD[0:3]	I 3.3V/5V -AUX	**Receive Data:** This is a group of 4 data signals aligned on nibble boundaries which are driven synchronous to the RXCLK by the external physical unit.

MAC Interface

Name	Pin Attr	Signal Description
TXEN	O 3.3V -AUX	**Transmit Enable:** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit
MDIO	I/O 3.3V/5V -AUX	**Management Data I/O:** Bi-direction signal used to transfer management information for the external physical unit. Requires external pull-up resistor.
RXDV	I 3.3V/5V -AUX	**Receive Data Valid**. This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data. This signal will encompass the frame, starting with the Start-Of-Frame delimiter and excluding the End-Of-Frame delimiter.
COL	I 3.3V/5V -AUX	**Collision Detect:** This signal is asserted high asynchronous by the external physical unit upon detection of a collision on the medium. It'll remain asserted as long as the collision condition persists.
CRS	I 3.3V/5V -AUX	**Carrier Sense:** This signal is asserted high asynchronously by the physical unit upon detection of a non-idle medium.
RXCLK	I 3.3V/5V -AUX	**Receive Clock** A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.
TXCLK	I 3.3V/5V -AUX	**Transmit Clock** A continuous clock that is sourced by the physical unit. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.

5.3 SiS961 MuTIOL Media I/O Controller

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attribute
VSS	0V	GROUND	Digital
VSSZ	0V	GROUND	Digital
IVDD	1.8V	MAIN	Digital
PVDDZ	1.8V	MAIN	Digital
VDDZ	1.8V	MAIN	Digital
VDDZCMP	1.8V	MAIN	Analog
VSSZCMP	0V	GROUND	Analog
ZVSSREF	0V	GROUND	Analog
PVDD	3.3V	MAIN	Digital
OVDD	3.3V	MAIN	Digital
VTT	1.1V-2.65V	MAIN	Digital
IVDD_AUX	1.8V	AUX	Digital
PVDD_AUX	3.3V	AUX	Digital
OVDD_AUX	3.3V	AUX	Digital
MIIAVDD	3.3V	AUX	Analog
MIIAVSS	0V	GROUND	Analog
USBVDD	3.3V	AUX	Analog
USBVSS	0V	GROUND	Analog
RTCVDD	3.3V	RTC	Analog
RTCVSS	0V	GROUND	Analog
Z1XAVDD	3.3V	MAIN	Analog
Z1XAVSS	0V	GROUND	Analog
Z4XAVDD	3.3V	MAIN	Analog
Z4XAVSS	0V	GROUND	Analog
IDEAVDD	1.8V	MAIN	Analog
IDEAVSS	0V	GROUND	Analog

General Purpose I/O

Signal Name	Pin Attr	Signal Description
GPIO[6:0]	I/O 3.3V/5V -M	**GPIO:** Can be a general purpose input or output.
GPIO14,[12:7]	I/O 3.3V/5V -AUX	**GPIO :** Can be a general purpose input or output.
GPIO13	O 3.3V/5V - AUX	**GPO:** Can be a general purpose output.
GPIO[18:15]	O 3.3V/5V - AUX	**GPO:** Can be a general purpose output.
GPIO[20:19]	I/O 3.3V/5V - AUX	**GPIO:** Can be a general purpose input or output.

5.4 SiS301LV / Chrontel CH7017 TV/LVDS Encoder

Pin #	Type	Symbol	Description
66,101	In/Out	**H1,H2**	**Horizontal Sync Input / Output** When the SYO control bit is low, these pins accept a horizontal sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a horizontal sync pulse 64 pixels wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
65,102	In/Out	**V1,V2**	**Vertical Sync Input / Output** When the SYO control bit is low, these pins accept a vertical sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 signal is the threshold level. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a vertical sync pulse one line wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
63,104	In	**DE1,DE2**	**Data Enable** These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF1 is the threshold level. One of these inputs is used by the LVDS links. The TV-Out function uses H and V sync signals and values in the SAV register as reference to active video.
62,105	Out	**FLD/STL1** **FLD/STL2**	**TV Field / Flat Panel Stall Signal** These outputs can be programmed to be either a TV Field output from the TV encoder or a Stall output from the flat panel Up-scaler. These outputs are tri-stated upon power up.
107	In/Out	**SPD**	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port, and uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
108	In	**SPC**	**Serial Port Clock Input** This pin functions as the clock input of the serial port and uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
106	In	**AS**	**Address Select** (Internal Pull-up) This pin determines the device address of the serial port.

Pin #	Type	Symbol	Description
112	In/Out	**SDD**	**Low-Voltage DDC Serial Data** Low-voltage serial data for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
113	In/Out	**SDC**	**Low-Voltage DDC Serial Clock** Low-voltage serial clock for DDC. It uses VREF2 / 2 as the threshold voltage. VREF2 divide by 2 function is generated on-chip.
114,116	In/Out	**DD1, DD2**	**DDC Serial Data** Serial data for DDC. (0V to 5V) .
111	In	**VREF2**	**Reference Voltage 2** Used to generate the threshold level for SDD, SDC, SPD and SPC port. This pin should be tied externally to the maximum voltage seen by the ports. (1.5V to 3.3V).
115,117	In/Out	**DC1,DC2**	**DDC Serial Clock** Clock for DDC. (0V to 5V)
123-126 56,57	In/Out	**GPIO[5:0]**	**General Purpose Input / Output [5:0]** These pins provide general purpose I/O and are controlled via the serial port. (3.3V).
127	Out	**ENAVDD**	**Panel Power Enable** Enable panel VDD. (3.3V)
128	Out	**ENABLK**	**Back Light Enable** Enable Back-Light of LCD Panel. (3.3V)
121	In	**HPD**	**Hot Plug Detect** (Internal Pull-down) This input pin determines whether a CRT monitor is connected to the VGA connector. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT* pin pulling low.
122	Out	**HPINT***	**Hot Plug Interrupt Output** This pin provides an open drain output, which pulls low when a termination change has been detected on the HPD input.
36	In	**VSWING**	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 35) using short and wide traces.
58	In	**RESET***	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

5.4 SiS301LV / Chrontel CH7017 TV/LVDS Encoder

Pin #	Type	Symbol	Description
2	Analog	**LPLLCAP**	**LVDS PLL Capacitor** This pins allows coupling of any signal to the on-chip loop filter capacitor.
5,24	Out	**LL2C,LL1C**	**Positive LVDS differential Clock2 & Clock1**
6,25	Out	**LL2C*,LL1C***	**Negative LVDS differential Clock2 & Clock1**
8,11,14,17	Out	**LDC[7:4]**	**Positive LVDS differential data[7:4]**
9,12,15,18	Out	**LDC[7:4]***	**Negative LVDS differential data[7:4]**
21,27,30,33	Out	**LDC[3:0]**	**Positive LVDS differential data[3:0]**
22,28,31,34	Out	**LDC[3:0]***	**Negative LVDS differential data [3:0]**
38	Analog	**ISET**	**Current Set Resistor Input** This pin sets the DAC current. A 140-ohm resistor should be connected between this pin and DAC_GND (pin 39) using short and wide traces.
40,42,44,46	Out	**DACB[3:0]**	**DAC Output B** Video Digital-to-Analog outputs.
41,43,45,47	Out	**DACA[3:0]**	**DAC Output A** Video Digital-to-Analog outputs.
120	Out	**VOUT**	**V-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
110	In	**VIN**	**V-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs.
119	Out	**HOUT**	**H-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
109	In	**HIN**	**H-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2.
49	Out	**C/HSYNC**	**Composite / Horizontal Sync** Provides composite sync in TV modes and horizontal sync in bypass RGB mode. This pin is driven by the DVDD supply.
50	Out	**BCO/VSYNC**	**Buffered Clock Outputs / Vertical Sync** This output pin provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply.

Pin #	Type	Symbol	Description
52	In	**XI/FIN**	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal (+ 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.
53	Out	**XO**	**Crystal Output** A parallel resonance 14.31818MHz crystal (+ 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
59	Out	**P-OUT**	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply (pin 60). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
61	In	**VREF1**	**Reference Voltage Input 1** The VREF1 pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
68-73,77-82	In	**D1[11:0]**	**Data1[11] through Data1[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
76,74	In	**XCLK1** **XCLK1***	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF1. The clock polarity can be selected by the MCP1 control bit.
85-90,94-99	In	**D2[11:0]**	**Data2[11] through Data2[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV. VREF1 is the threshold level.
93,91	In	**XCLK** **XCLK2***	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF1. The clock polarity can be selected by the MCP2 control bit.

5.4 SiS301LV / Chrontel CH7017 TV/LVDS Encoder

Pin #	Type	Symbol	Description
118	**Power**	**V5V**	**5V supply for H/VOUT** (5V)
64,83,84,103	**Power**	**DVDD**	**Digital Supply Voltage (3.3V)**
67,75,92,100	**Power**	**DGND**	**Digital Ground**
60	**Power**	**VDDV**	**I/O Supply Voltage** (1.1V to 3.3V)
55	**Power**	**TVPLL_VDD**	**TV PLL Supply Voltage** (3.3V)
54	**Power**	**TVPLL_VCC**	**TV PLL Supply Voltage** (3.3V)
51	**Power**	**TVPLL_GND**	**TV PLL Ground**
37	**Power**	**DAC_VDD**	**DAC Supply Voltage** (3.3V)
39,48	**Power**	**DAC_GND**	**DAC Ground**
7,13,19,20,26,32	**Power**	**LVDD**	**LVDS Supply Voltage** (3.3V)
4,10,16,23,29,35	**Power**	**LGND**	**LVDS Ground**
1	**Power**	**LPLL_VDD**	**LVDS PLL Supply Voltage** (3.3V)
3	**Power**	**LPLL_GND**	**LVDS PLL Ground**

5.5 MB86613L IEEE1394 Controller

PCI Bus Interface

Name of pin	I/O	Function
PCICLK	I	PCI bus clock input pin (Max. 33MHz)
RST#	I	System reset input pin.
AD[31:0]	I/O	32-bit PCI Address/Data multiplexed pins.
C/BE#[3:0]	I/O	PCI Bus Command/Byte Enable multiplexed pins.
PAR	I/O	Even Parity pin for AD[31:0] and C/BE#[3:0]. This pin state becomes valid after 1 PCICLK.
FRAME#	I/O	Frame signal pin that indicates the PCI bus is driven by the master.
IRDY#	I/O	Data Ready signal pin for bus master device.
TRDY#	I/O	Data Ready signal pin for target device.
STOP#	I/O	Stop signal pin for the data transfer from target to master.
IDSEL	I	Chip select pin to access the configuration register.
DEVSEL	I/O	Device select pin. While the device is a target, this pin outputs the select signal that indicates the self device is selected. While the device is a master, this pin functions as an input pin to indicate that a device on the bus is selected.
REQ#	O	Request signal output pin to the bus arbiter to request for the PCI bus use.
GNT#	I	Grant signal input pin from the bus arbiter to receive the response to the REQ# signal.
PERR#	I/O	Data Parity Error input/output pin.
SERR#	OD	Address Parity Error output pin. (Open-drain type output pin.)
INTA#	OD	Interrupt output pin. (Open-drain type output pin.)
PME#	O	PCI power management enable.

Memory Interface

Name of pin	I/O	Function
EEDI	O	Data output pin for EEPROM device.
EEDO	I	Data input pin for EEPROM device.
EECS	O	Chip Select pin to select the externally connected EEPROM device.
EECLK	O	Clock output pin for EEPROM device.

1394 Interface

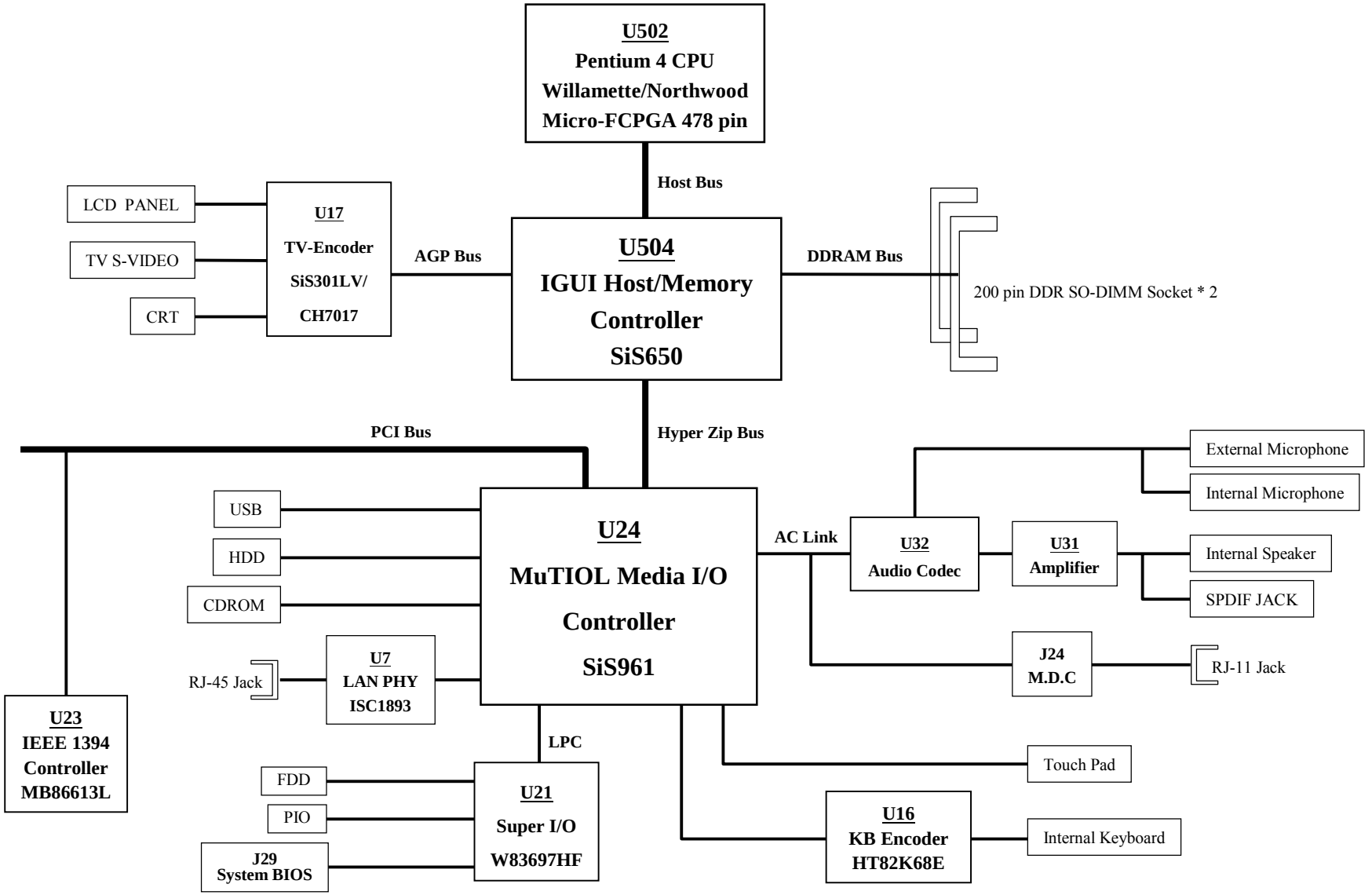
Name of pin	I/O	Function
TPA	I/O	TPA positive signals of 1394 cable port.
TPB	I/O	TPB positive signals of 1394 cable port.
TPA#	I/O	TPA negative signals of 1394 cable port
TPB#	I/O	TPB negative signals of 1394 cable port.
TPBIAS	O	TP Bias voltage supply pin.
CPS	I	Cable Power input pin.
RO	O	Load resistance connection pin (Connect with GND via a 5.1k resistor)

Others

Name of pin	I/O	Function
X1(CLK), X0	I	Clock input pin for the on-chip PLL (24.576MHz) or Crystal oscillator pins.
RF	O	Connect this pin with GND via a 5.1k resistor.
FIL	O	Filter circuit connection pin.
TEST	I	This pin is used for the test mode. Normally connect this pin with GND.
N.C.	-	Non-connection pins. Do not connect with these pins.

8500 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of long reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Signon messages displayed

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

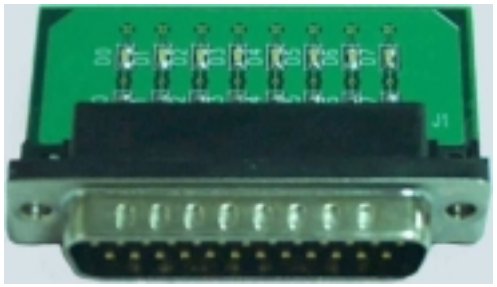
8500 N/B Maintenance

7.3 Maintenance Diagnostics

7.3.1 Diagnostic Tools :

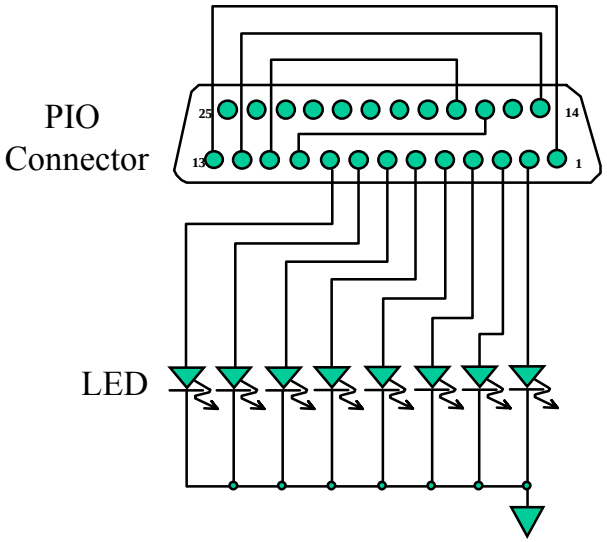
- **LED * 8**
- **PIO CONNECTOR * 1**

OR



P/N:411904800001
Description: PWA; PWA-378Port Debug BD
Note: Order it from MIC/TSSC

7.3.2 Circuit:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

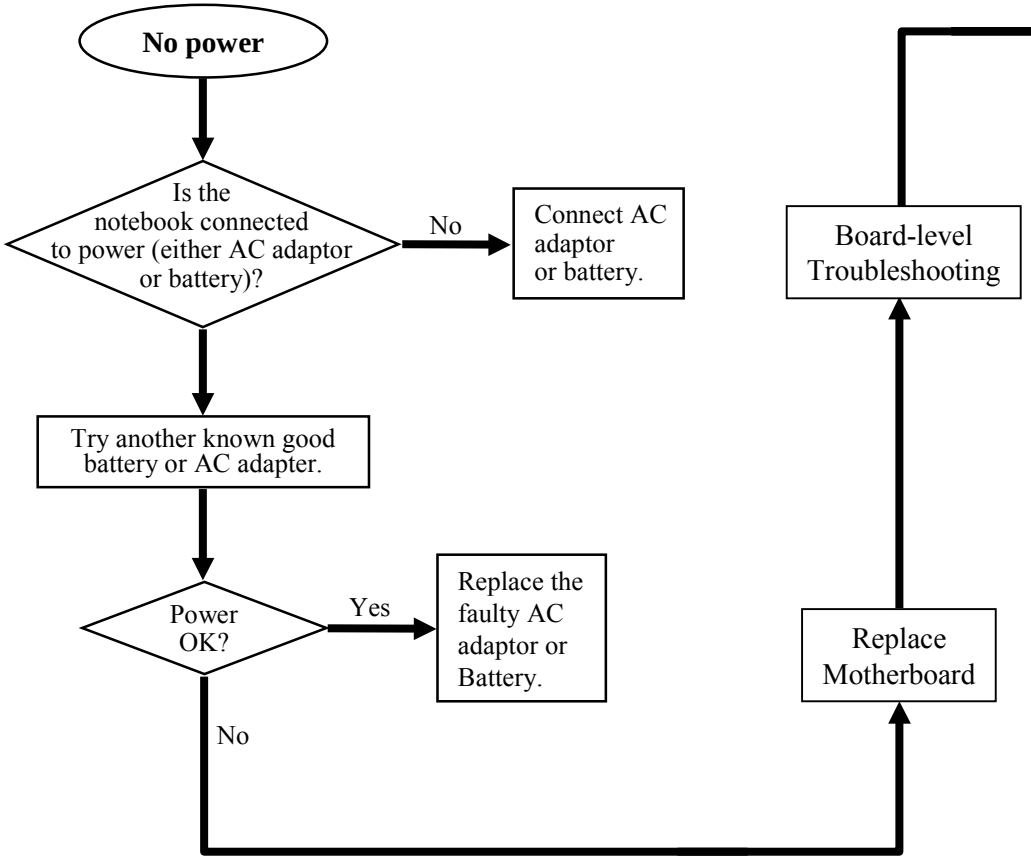
PIN{9:2}: PD{7:0}

8. Trouble Shooting

8500 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

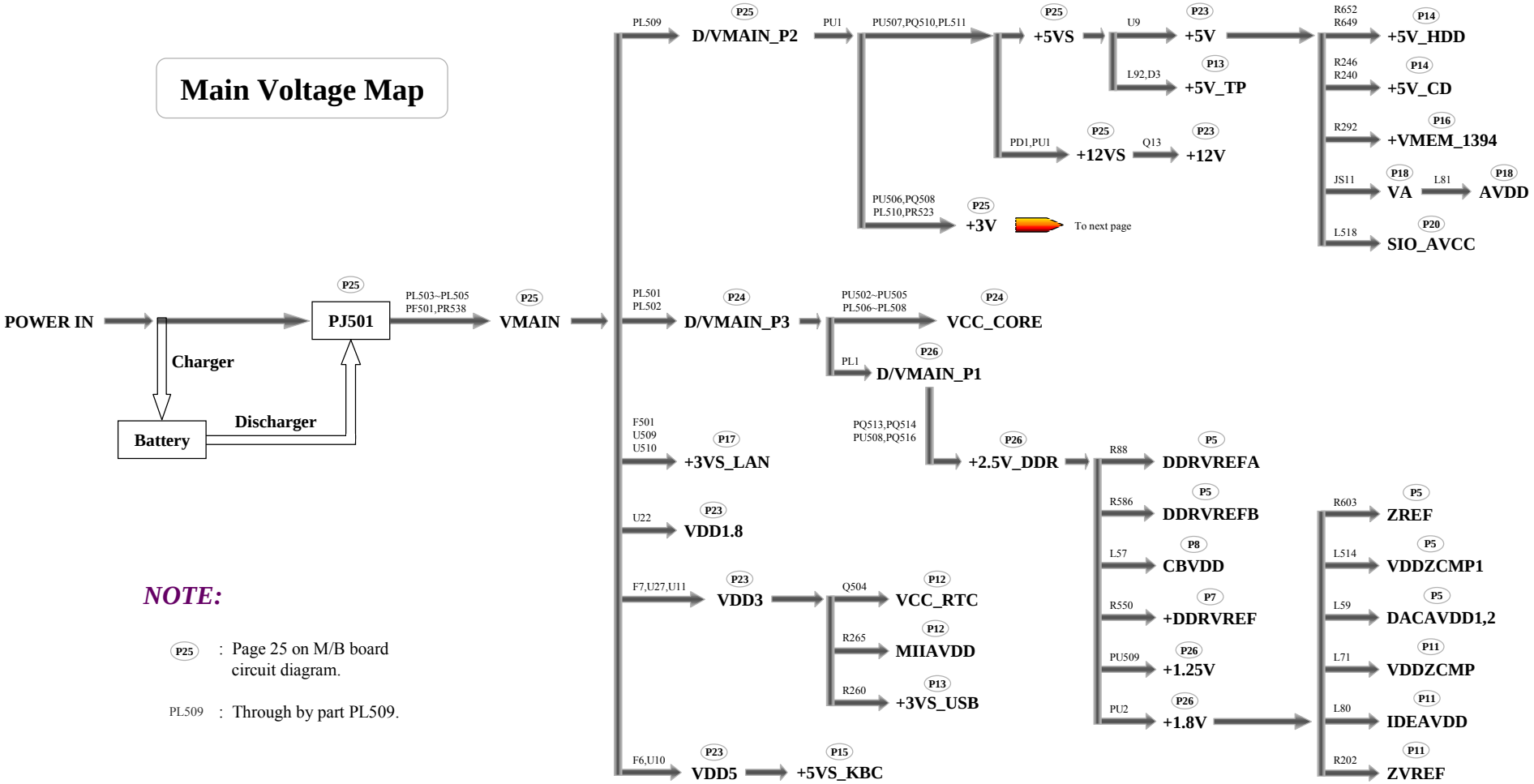
Parts:	**Signals:**
PJ501	VMAIN
PU510	EMC_PWRBTN#
PU511	PWR_ON
PU501	961_PWRBTN#
U21	PSON#
U24	+12VS
U16	+5VS
PU508	+3V
PU1	VDD5
U10	VDD3
U27	VDD1.8
U11	+2.5V_DDR
U22	+1.8V
U509	+1.25V
U30	

8500 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



NOTE:

P25 : Page 25 on M/B board circuit diagram.

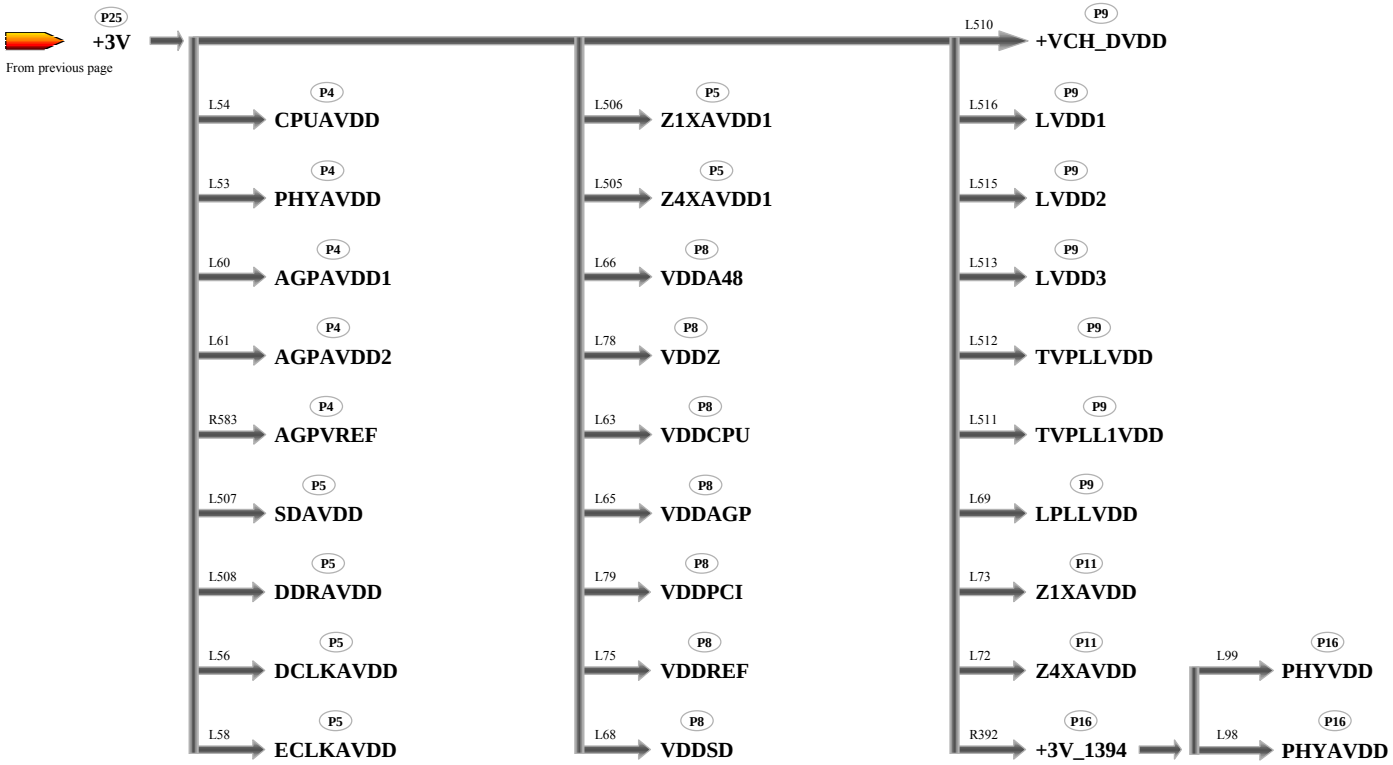
PL509 : Through by part PL509.

8500 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

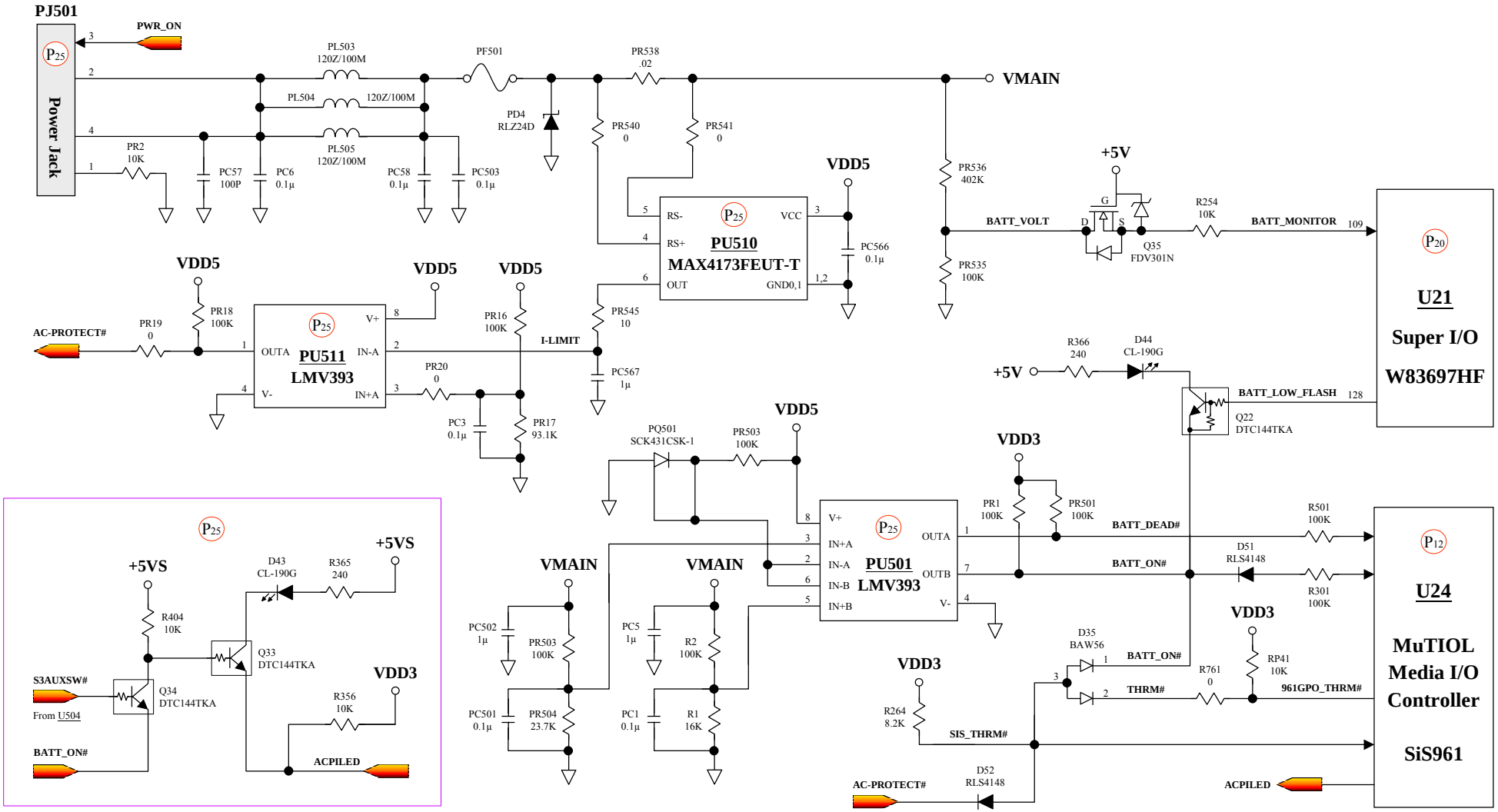
Main Voltage Map



8500 N/B Maintenance

8.1 No Power – VMAIN

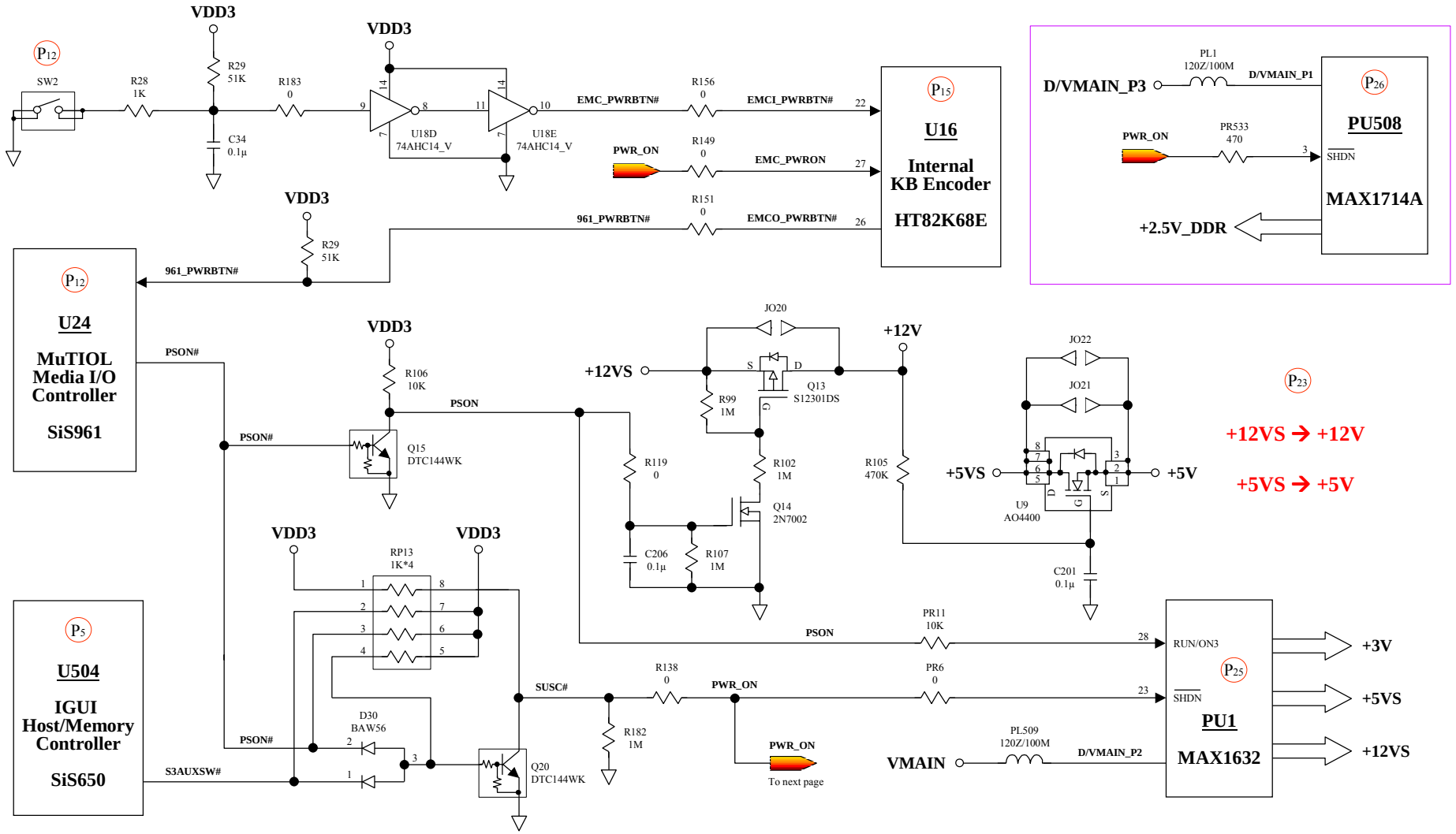
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8500 N/B Maintenance

8.1 No Power – +3V/+5V/+12V/+2.5V_DDR

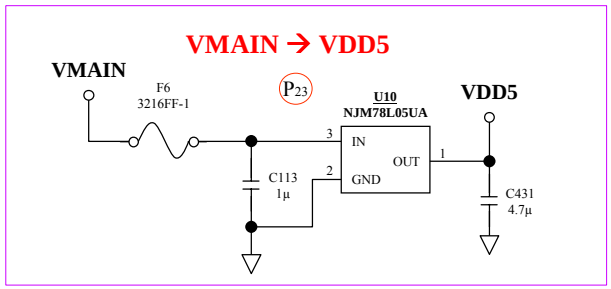
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

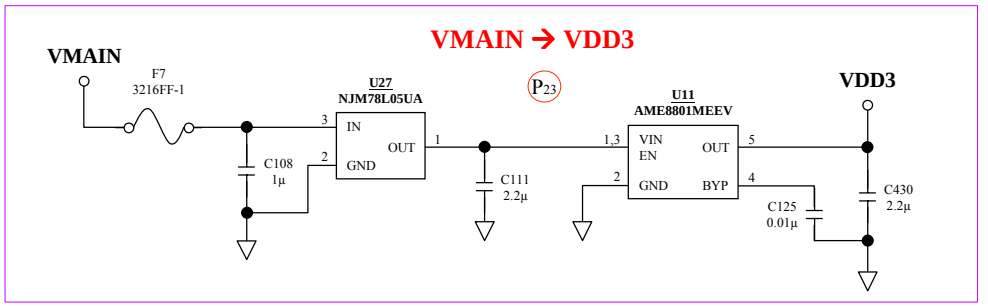


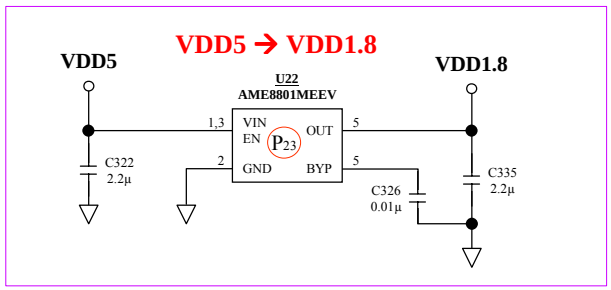
8500 N/B Maintenance

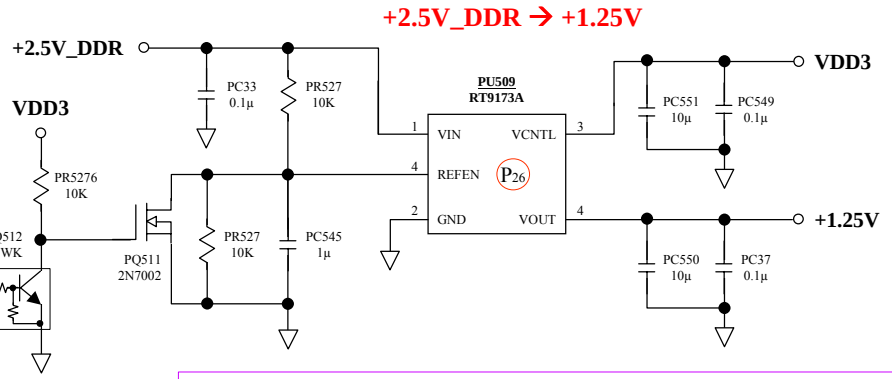
8.1 No Power – VDD5/VDD3/VDD1.8/+1.8V/+1.25V

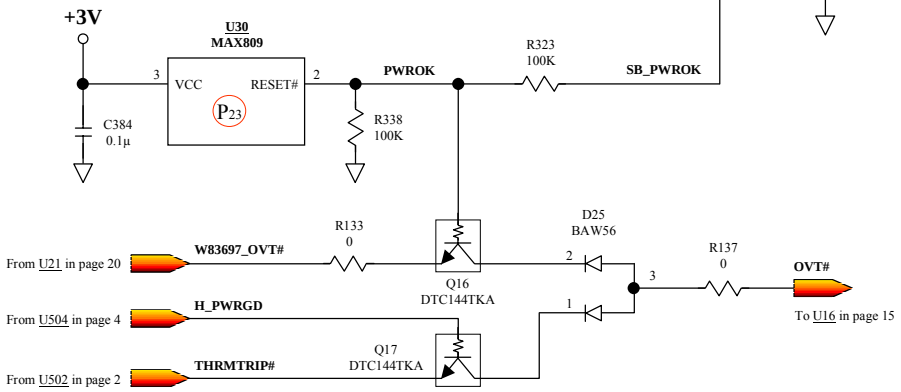
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

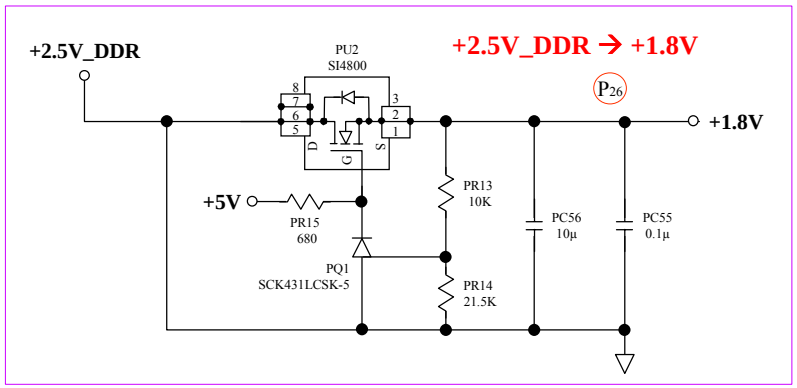






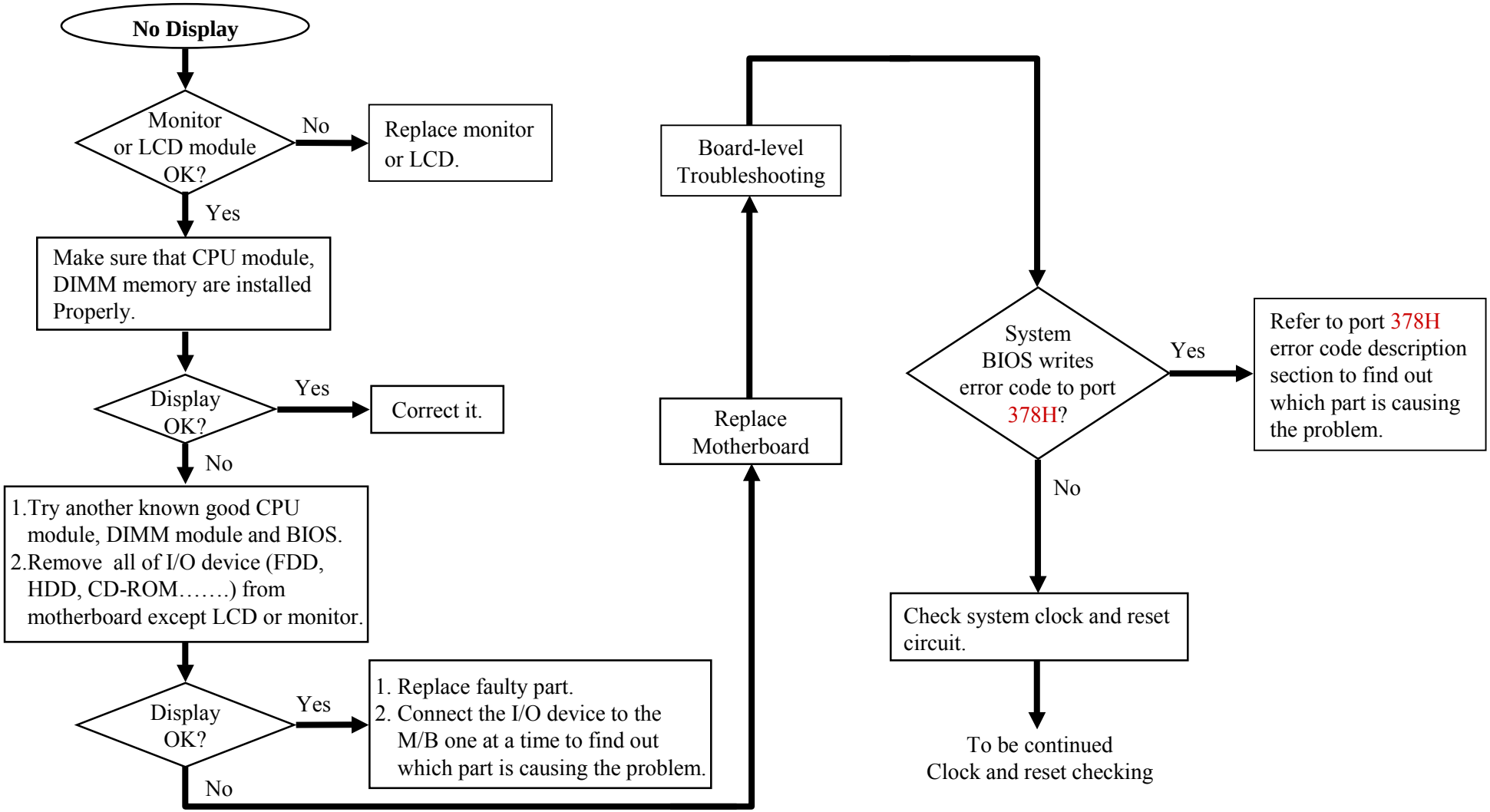






8.2 No Display

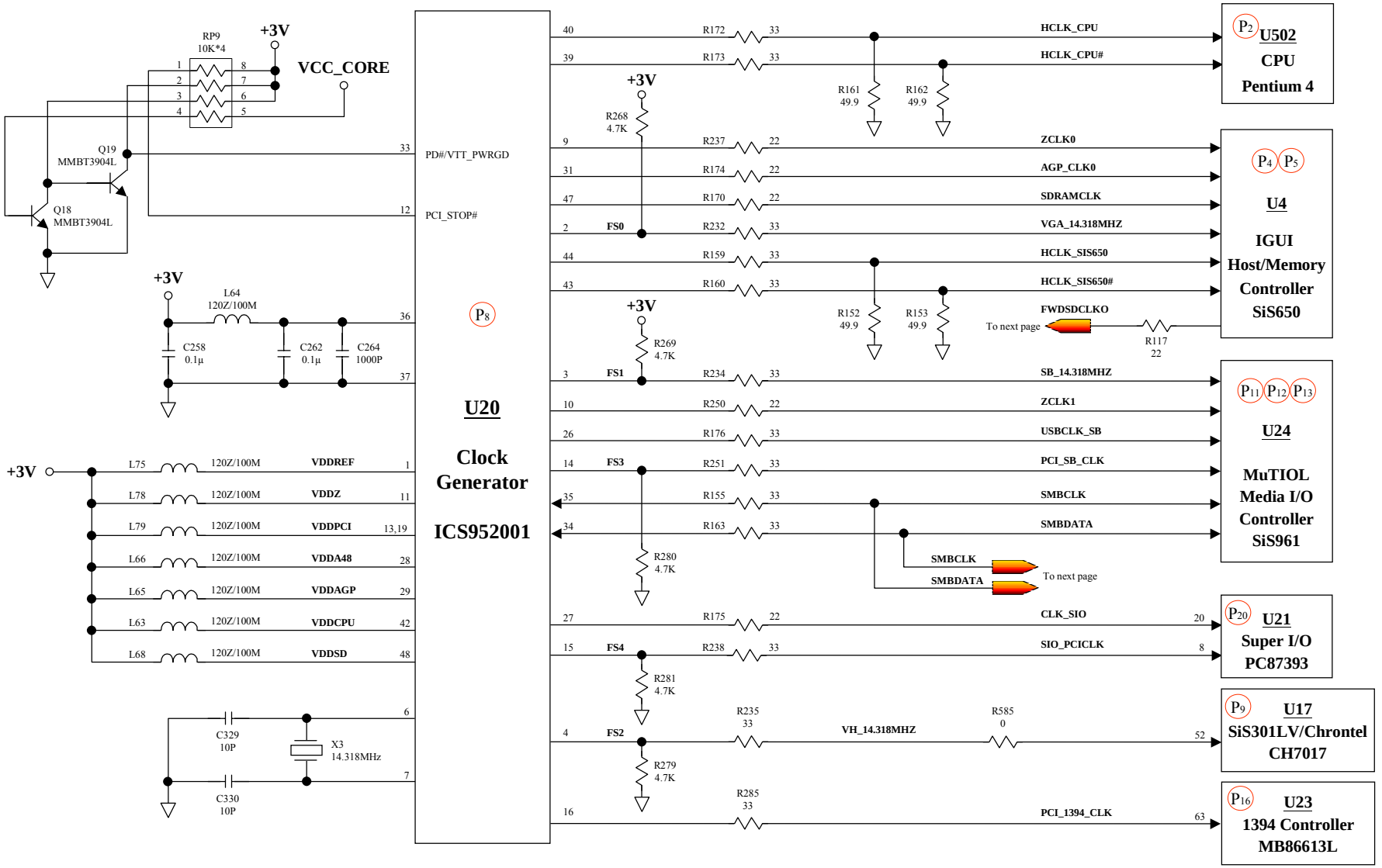
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



8500 N/B Maintenance

8.2 No Display

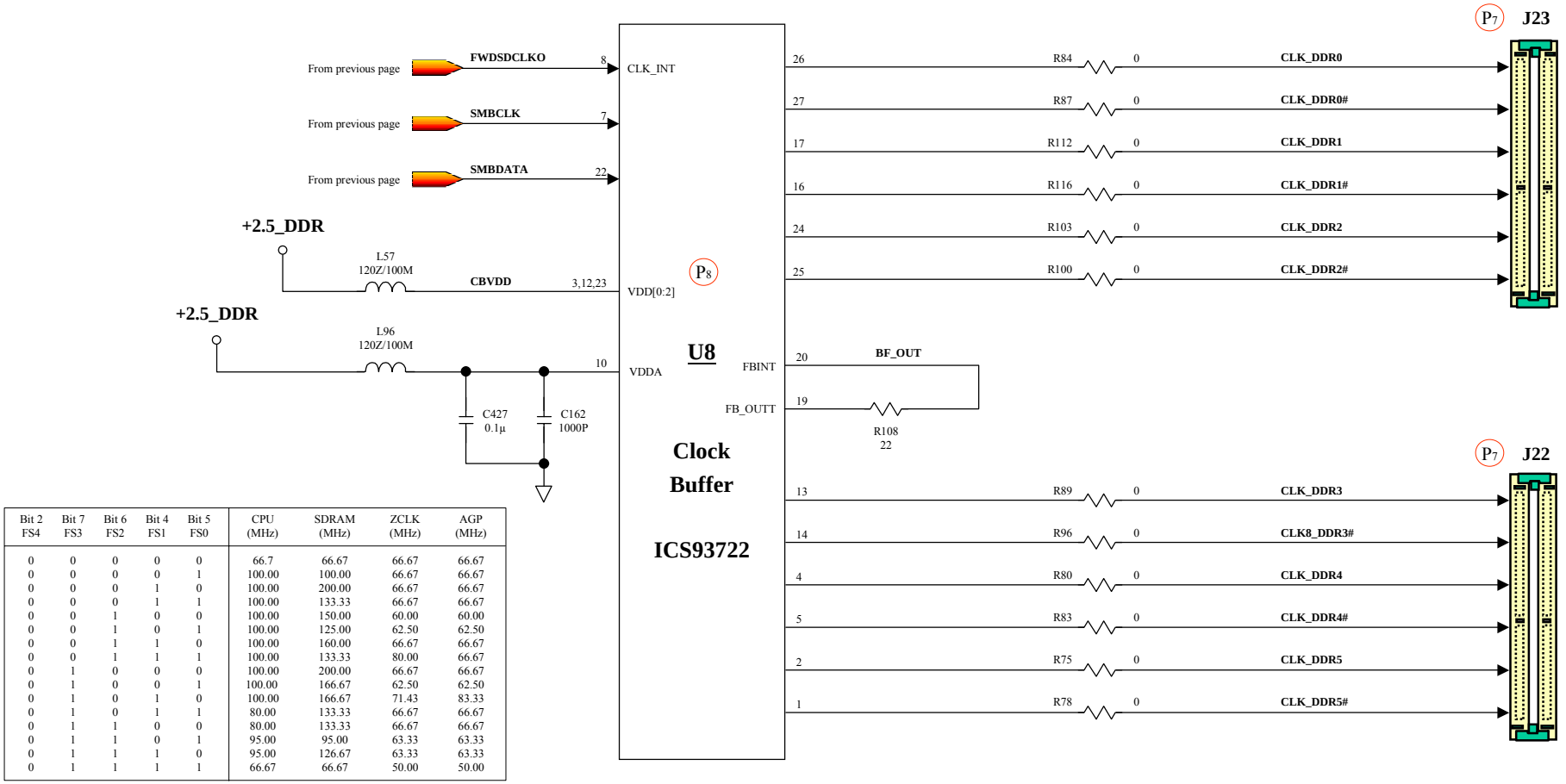
****** System Clock Check ******



8500 N/B Maintenance

8.2 No Display

****** System Clock Check ******

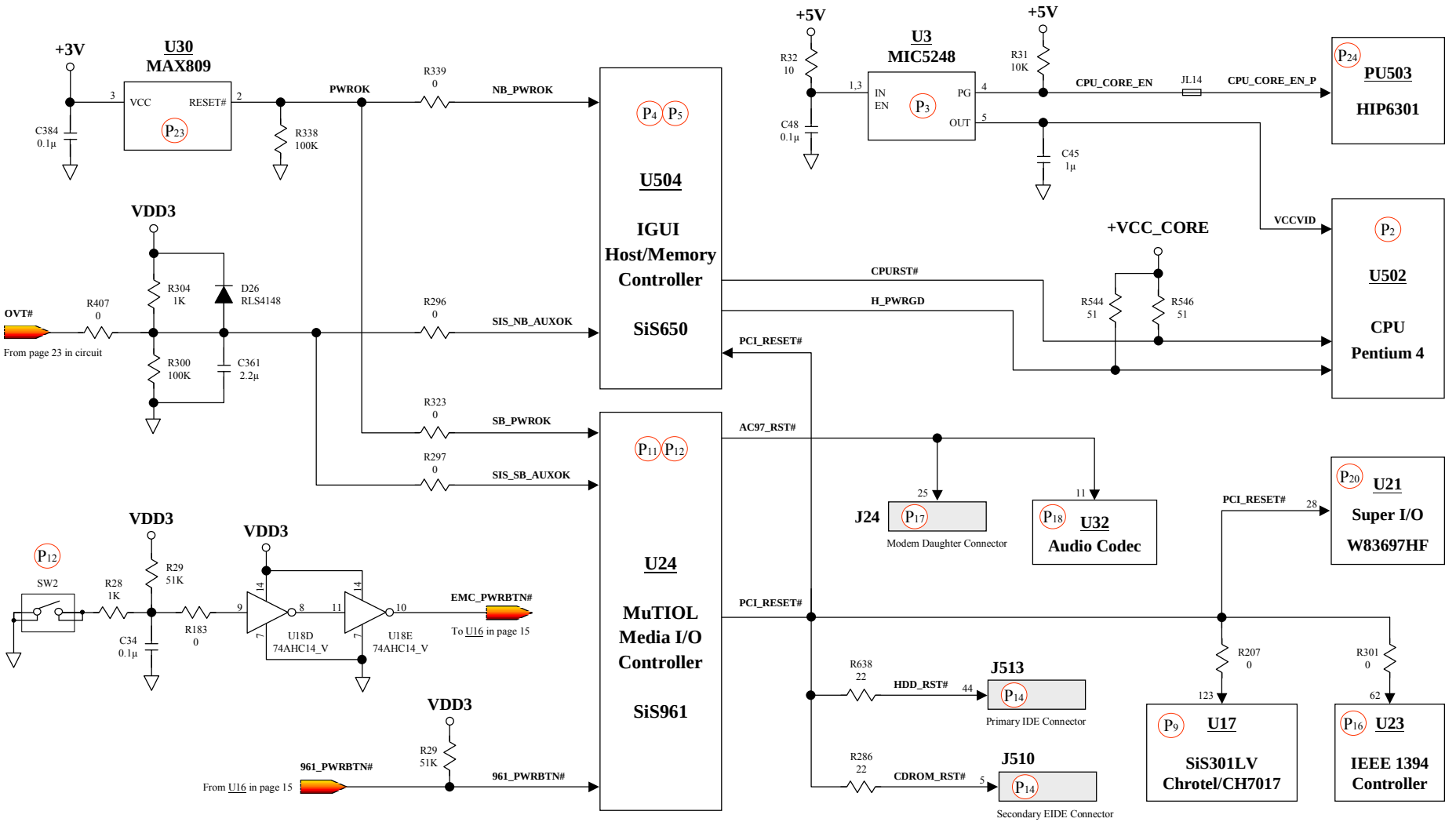


Bit 2 FS4	Bit 7 FS3	Bit 6 FS2	Bit 4 FS1	Bit 5 FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz)
0	0	0	0	0	66.7	66.67	66.67	66.67
0	0	0	0	1	100.00	100.00	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	100.00	150.00	60.00	60.00
0	0	1	0	1	100.00	125.00	62.50	62.50
0	0	1	1	0	100.00	160.00	66.67	66.67
0	0	1	1	1	100.00	133.33	80.00	66.67
0	1	0	0	0	100.00	200.00	66.67	66.67
0	1	0	0	1	100.00	166.67	62.50	62.50
0	1	0	1	0	100.00	166.67	71.43	83.33
0	1	0	1	1	80.00	133.33	66.67	66.67
0	1	1	0	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	1	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

8500 N/B Maintenance

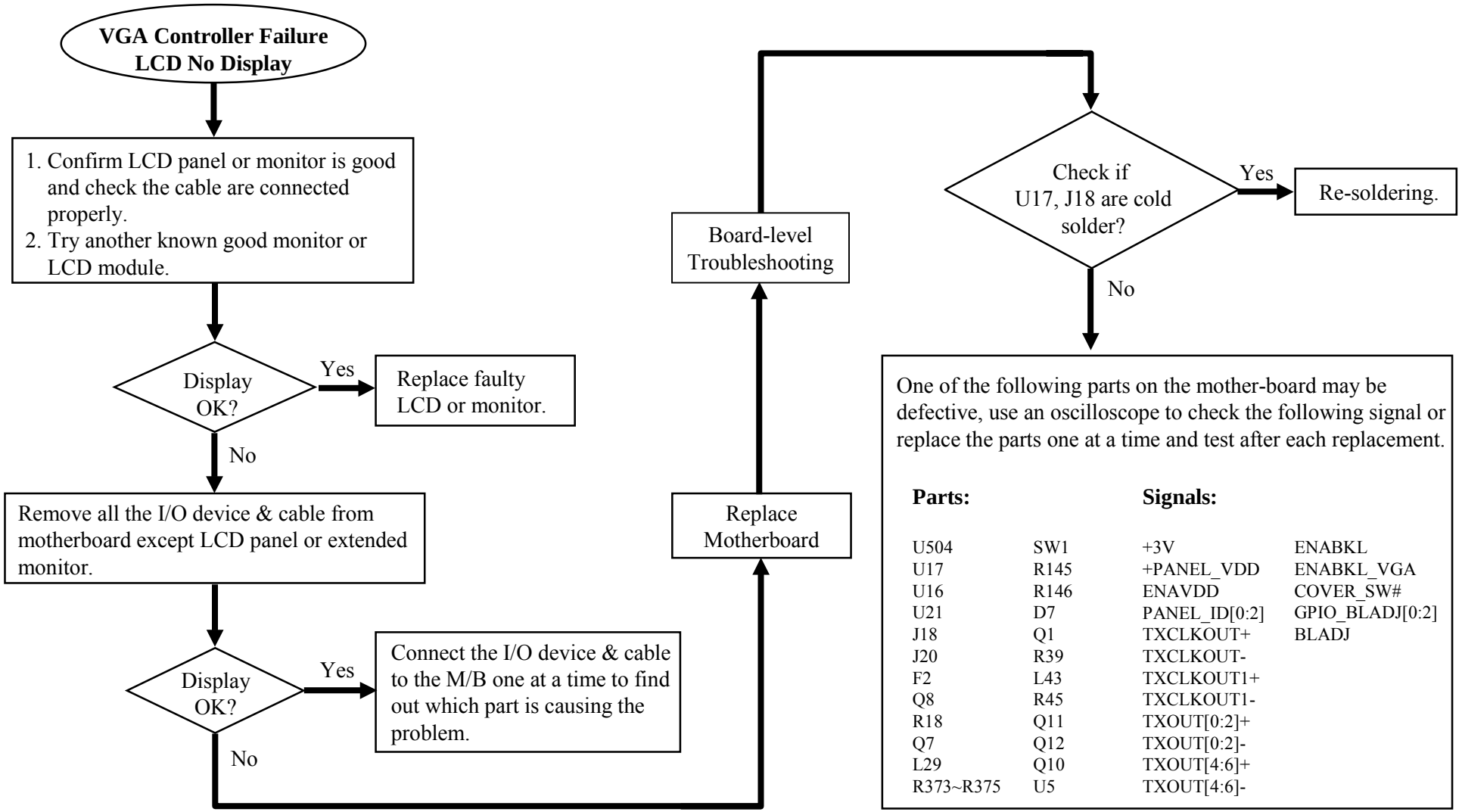
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

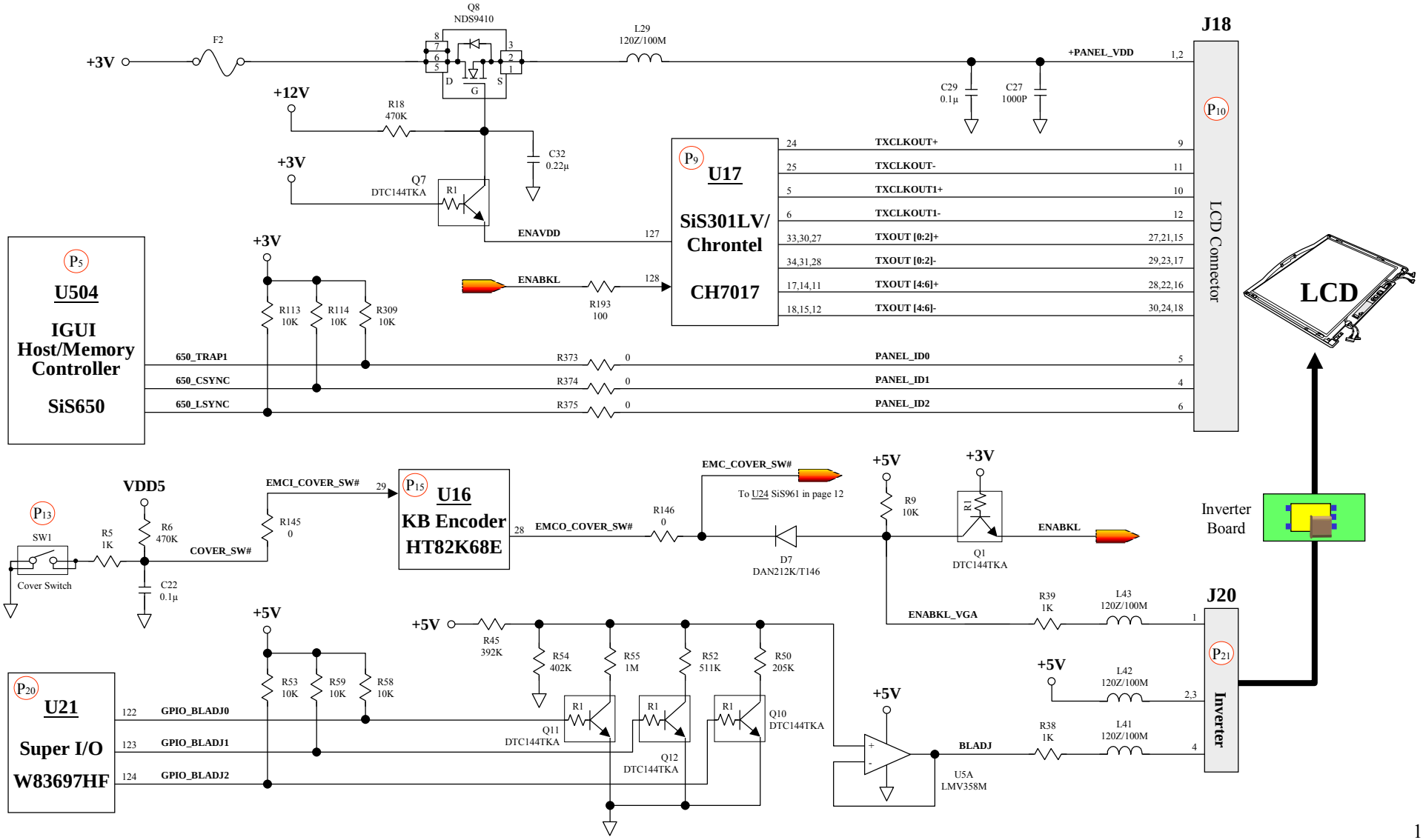
There is no display or picture abnormal on LCD although power-on-self-test is passed.



8500 N/B Maintenance

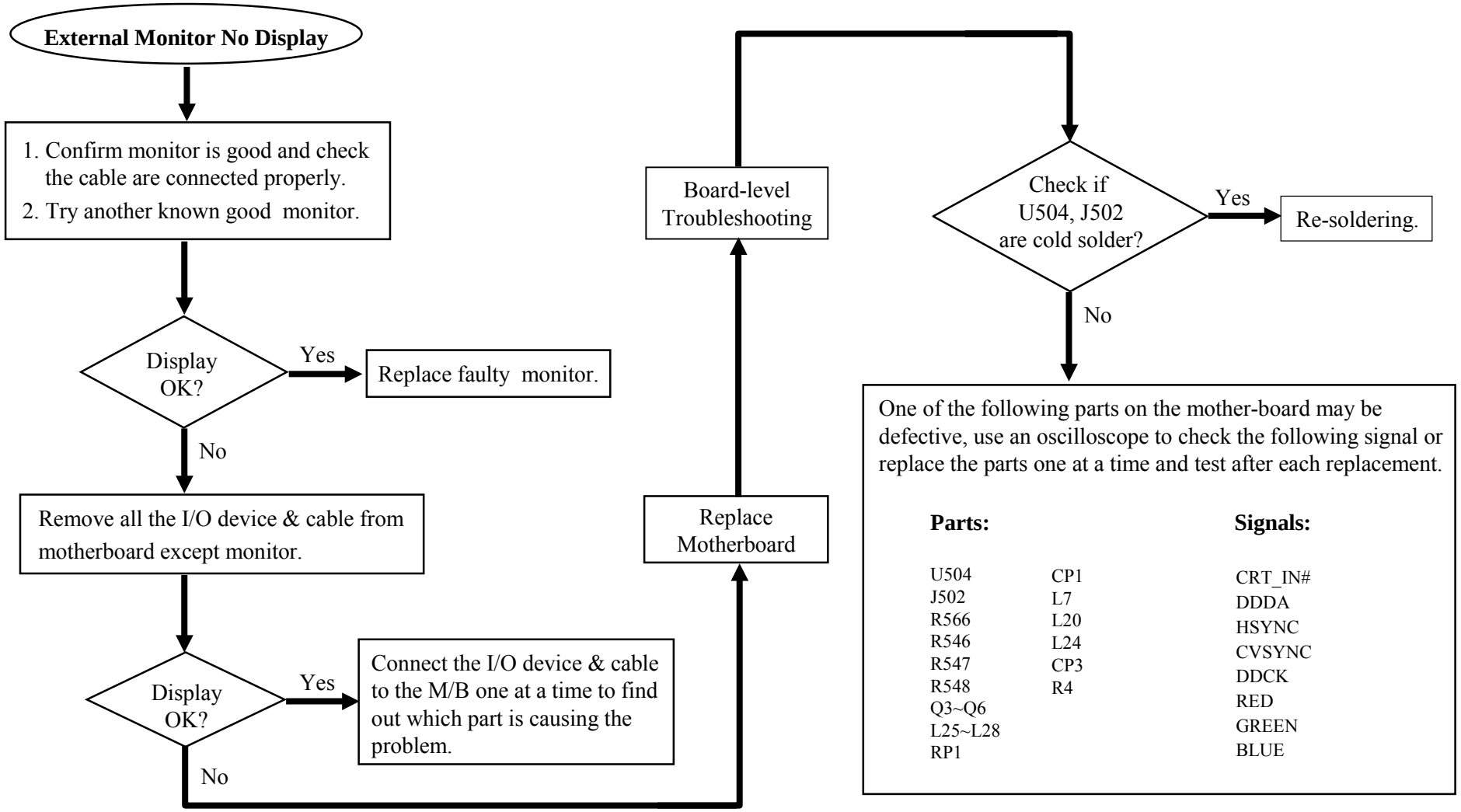
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



8.4 External Monitor No Display

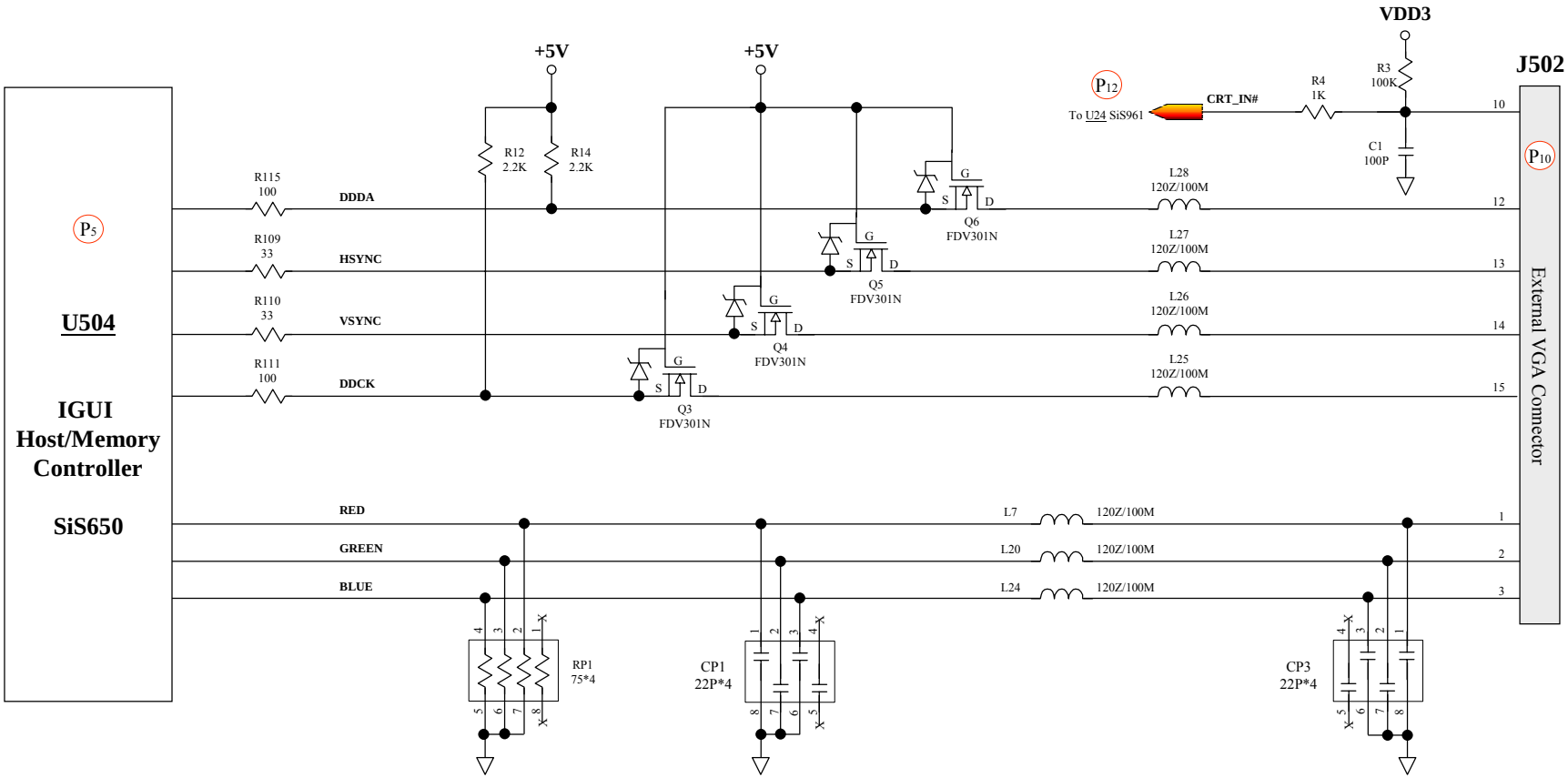
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8500 N/B Maintenance

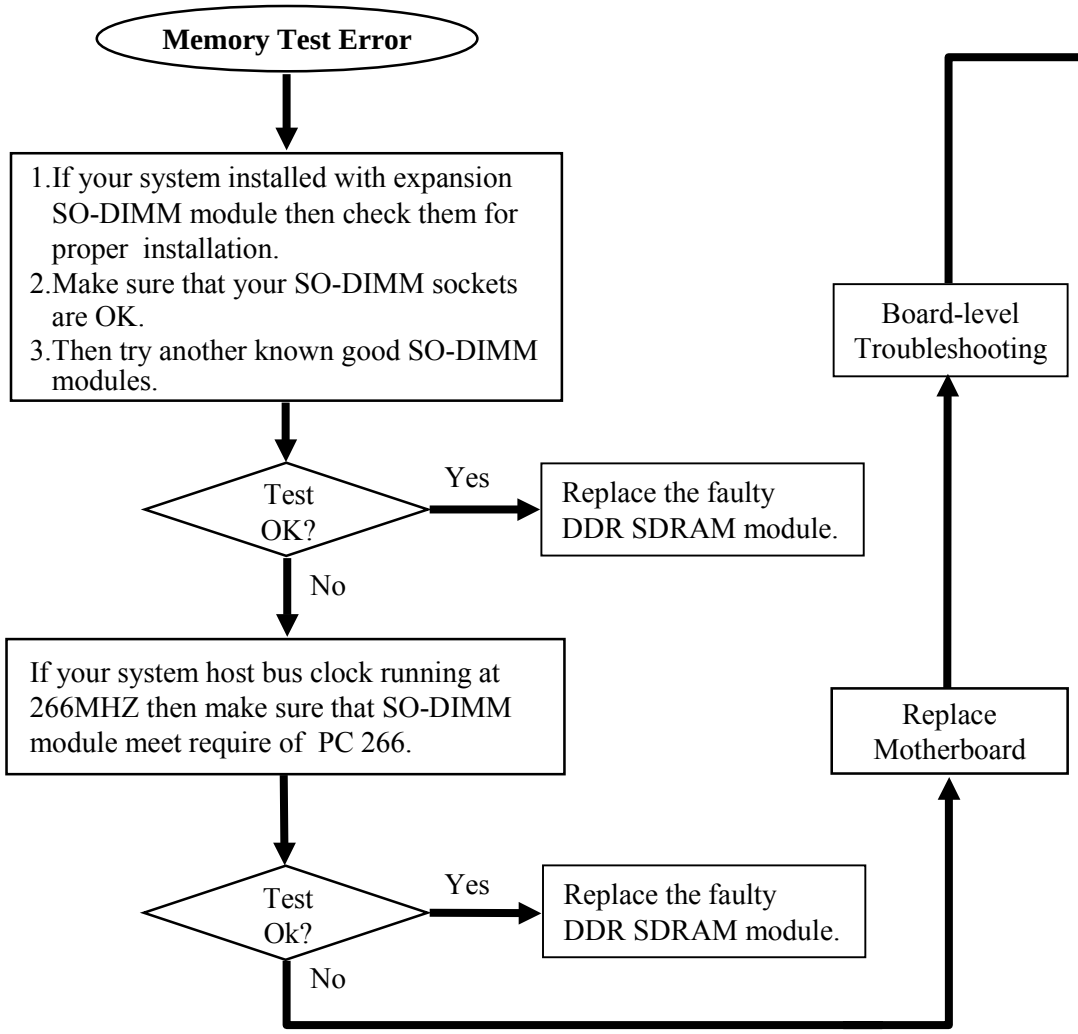
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Extend DDR SDRAM is failure or system hangs up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

U504
U20
U8
J23
J22
L508
RP538~RP547
RP507
RP509
RP510
RP512
RP514
RP518
RP520
RP522
RP524
RP526~RP529
R143
R632
R117
R155
R163
R84
R112
R103
R87
R116
R100
R89
R80
R75
R96
R83
R78

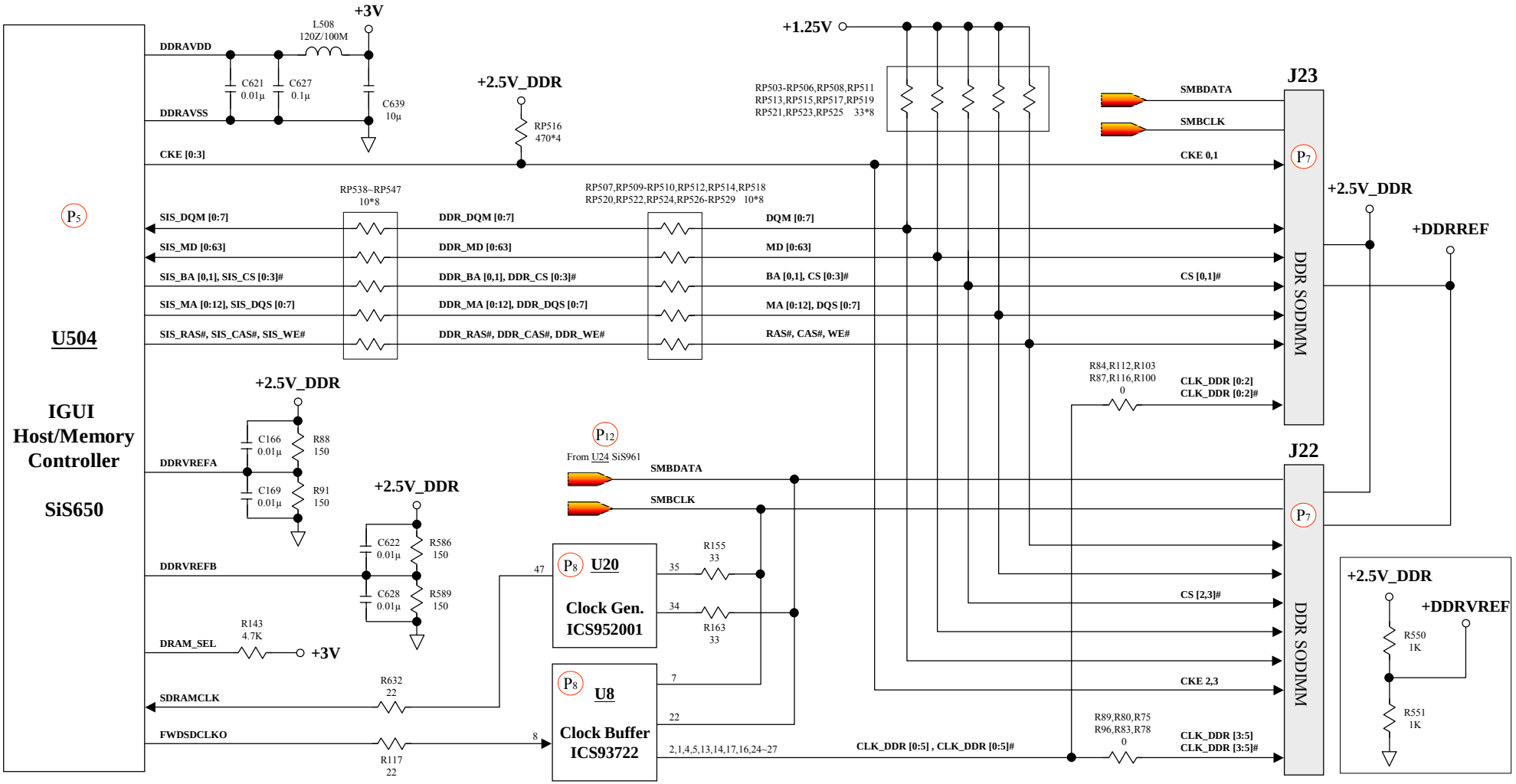
Signals:

+3V
+2.5V_DDR
+DDRVREF
DDRAVDD
CKE[0:3]
SIS_DQM[0:7]
SIS_MD[0:63]
SIS_BA [0,1]
SIS_CS[0:3]#
SIS_MA[0:12]
SIS_DQS[0:7]
SIS_RAS#
SIS_CAS#
SIS_WE#
DDRVREFA
DDRVREFB
DRAM_SEL
SDRAMCLK
FWDSDCLK
SMBCLK
SMBDATA
CLK_DDR[0:5]
CLK_DDR[0:5]#

8500 N/B Maintenance

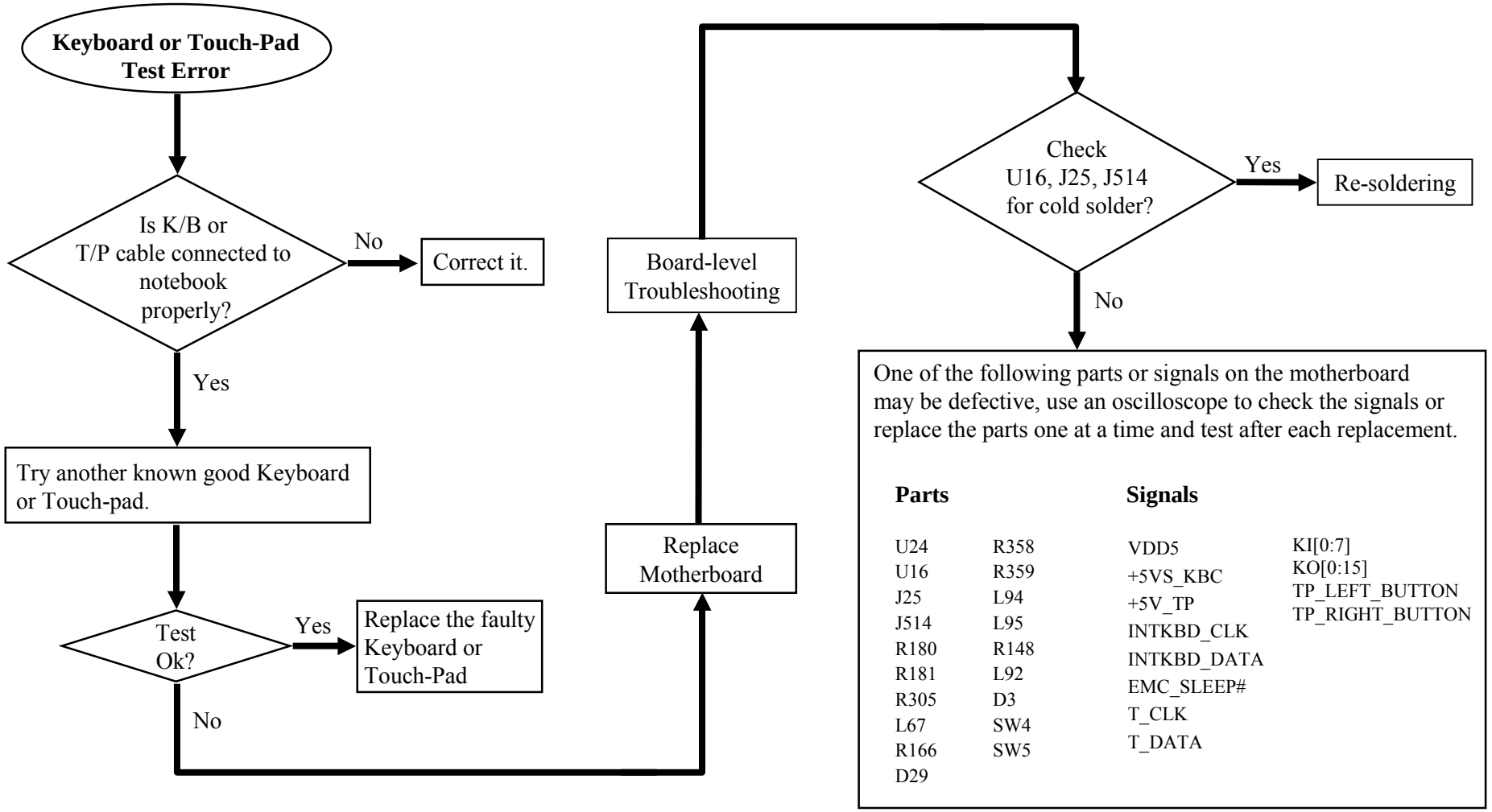
8.5 Memory Test Error

Extend DDR SDRAM is failure or system hangs up.



8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



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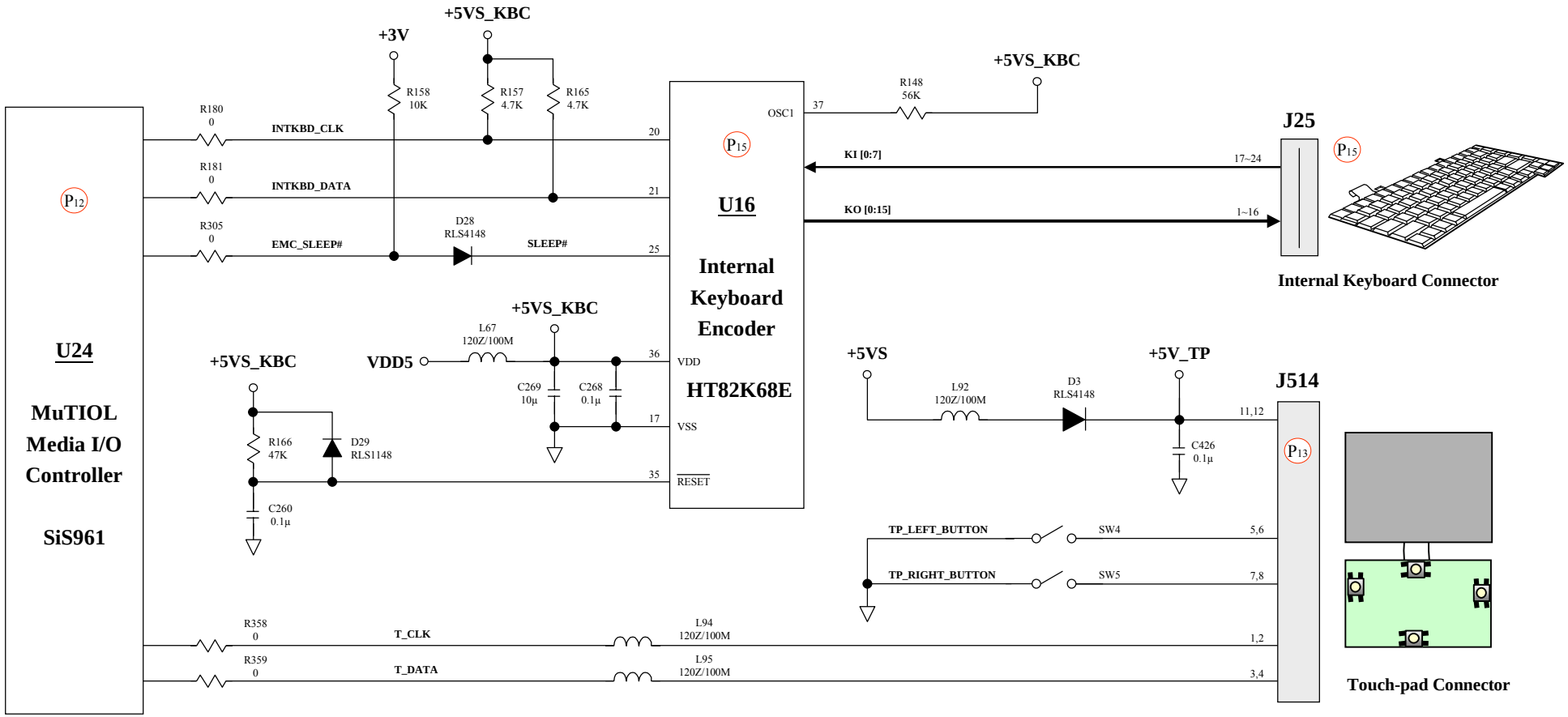
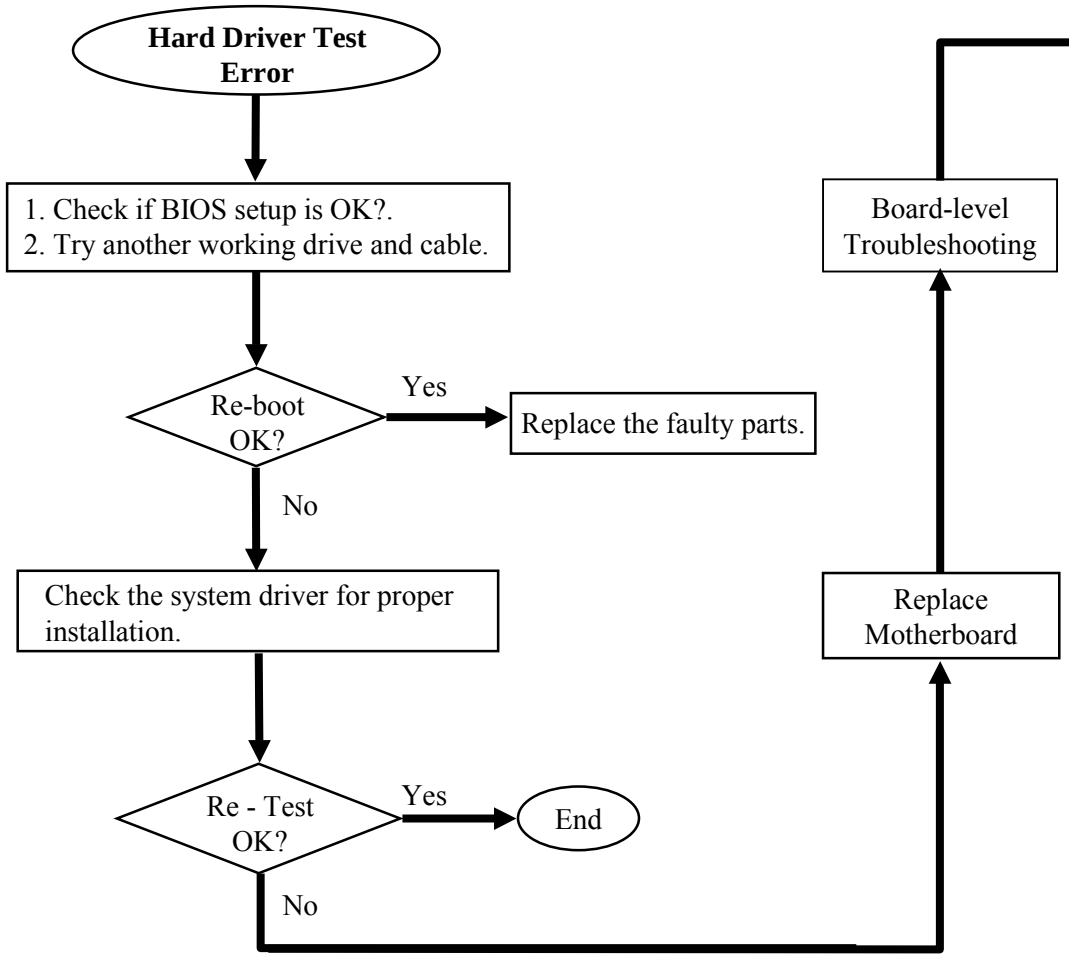
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U24	+5V
J513	+5V_HDD
L80	+1.8V
R652	IDEAVDD
R169	IDE_PIORDY
R638	PCI_RESET#
RP25	IDE_PDD[0:15]
RP26	IDE_PDA[0:2]
RP29	IDE_PDCS3#
RP30	IDE_PDCS1#
RP33	IDE_PDIOR#
RP36	IDE_PDIOW#
RP39	IDE_PDDACK#
R368	IDE_PDDREQ
D46	IDE_IRQ14

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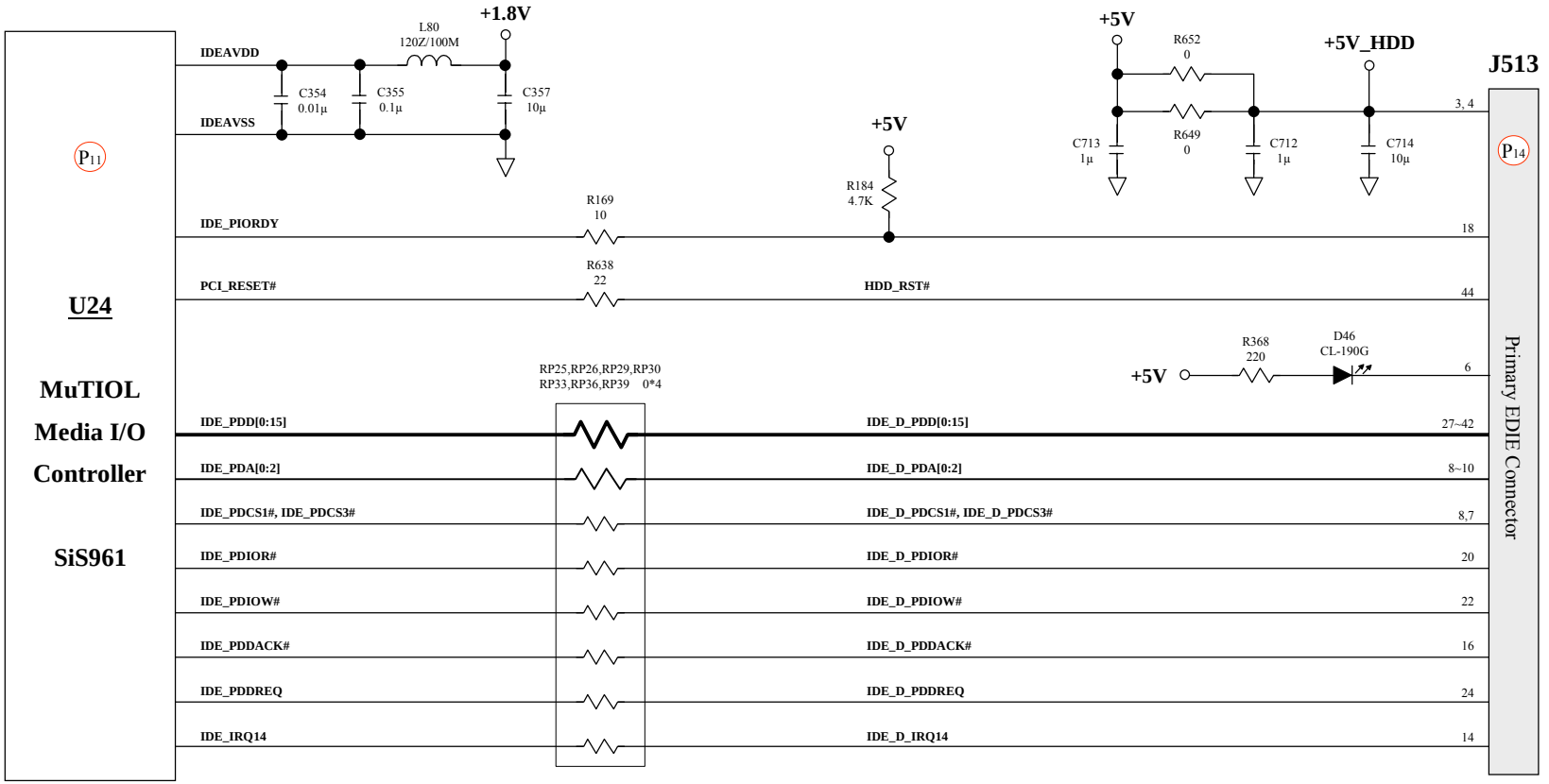
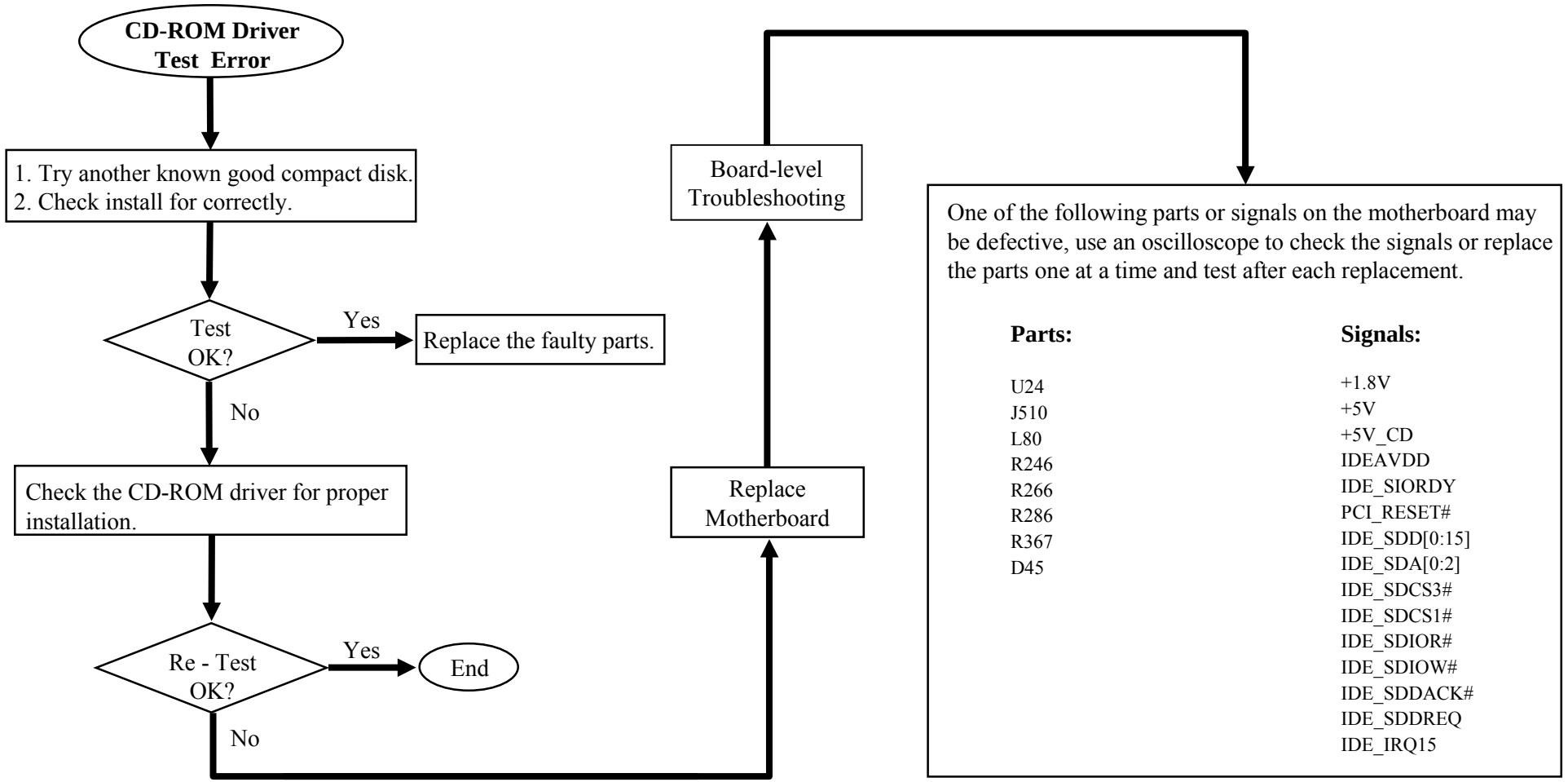
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



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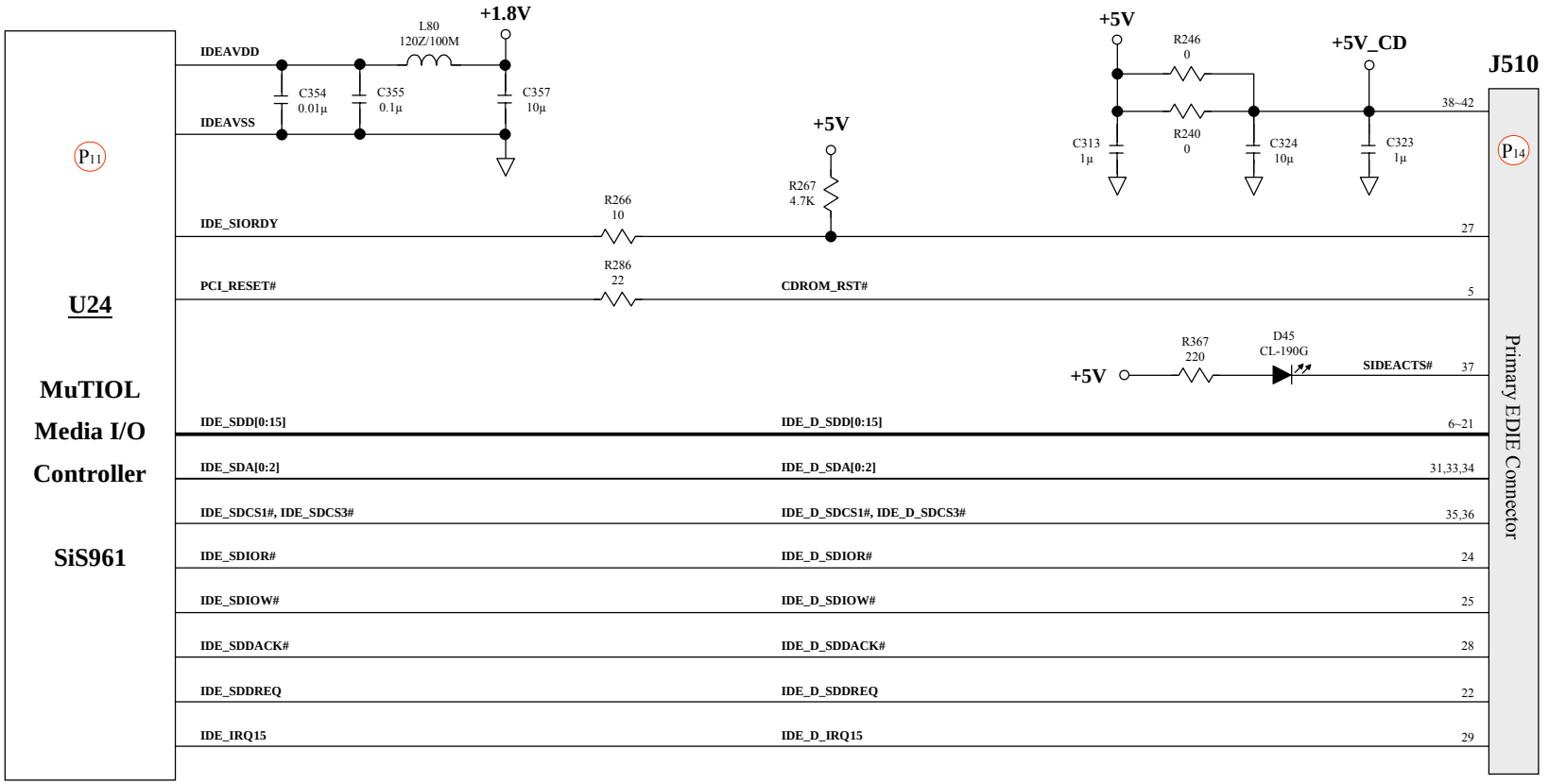
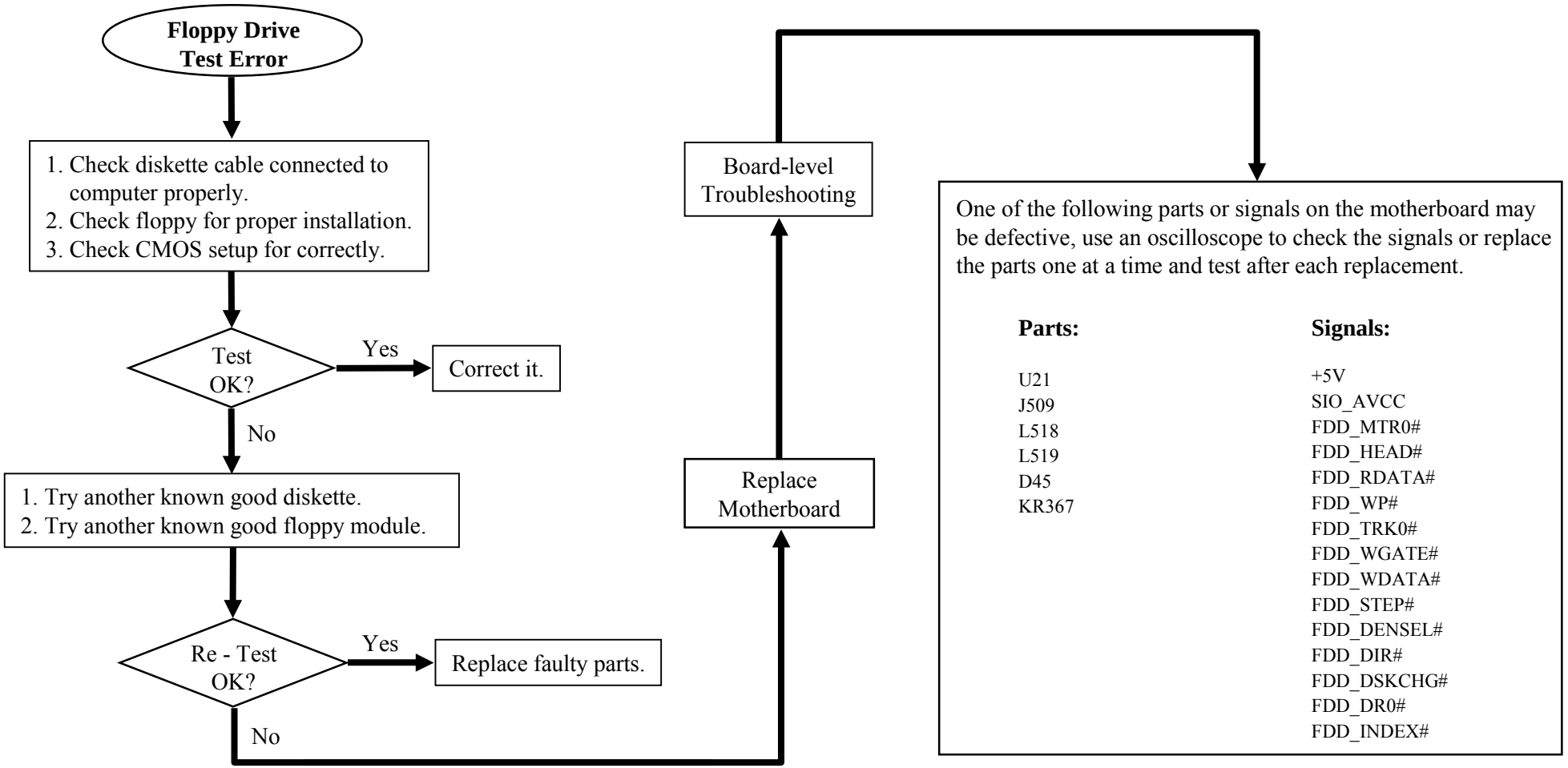
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



8.9 Floppy Drive Test Error

An error message is shown when loading data from disk to system.



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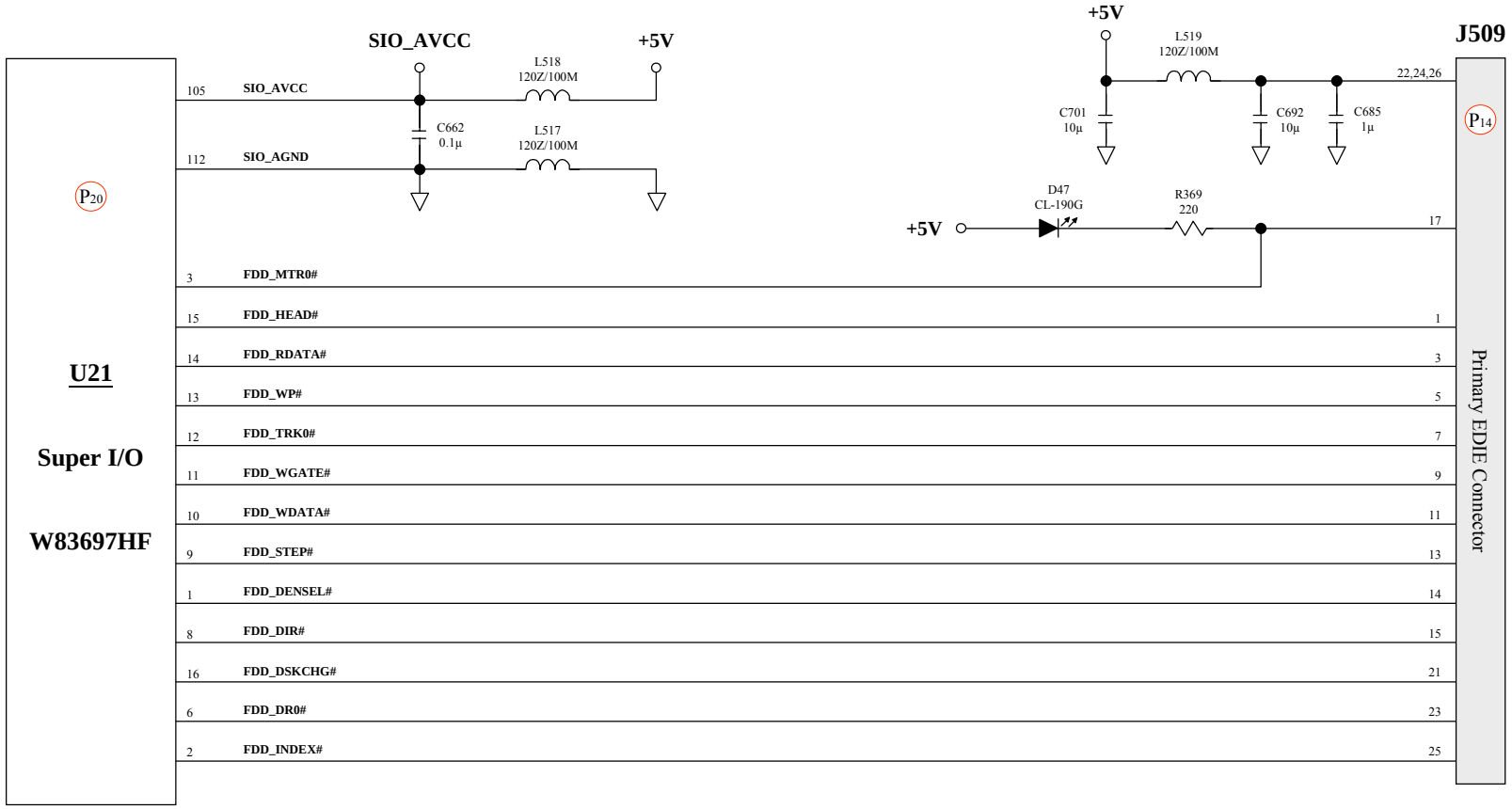
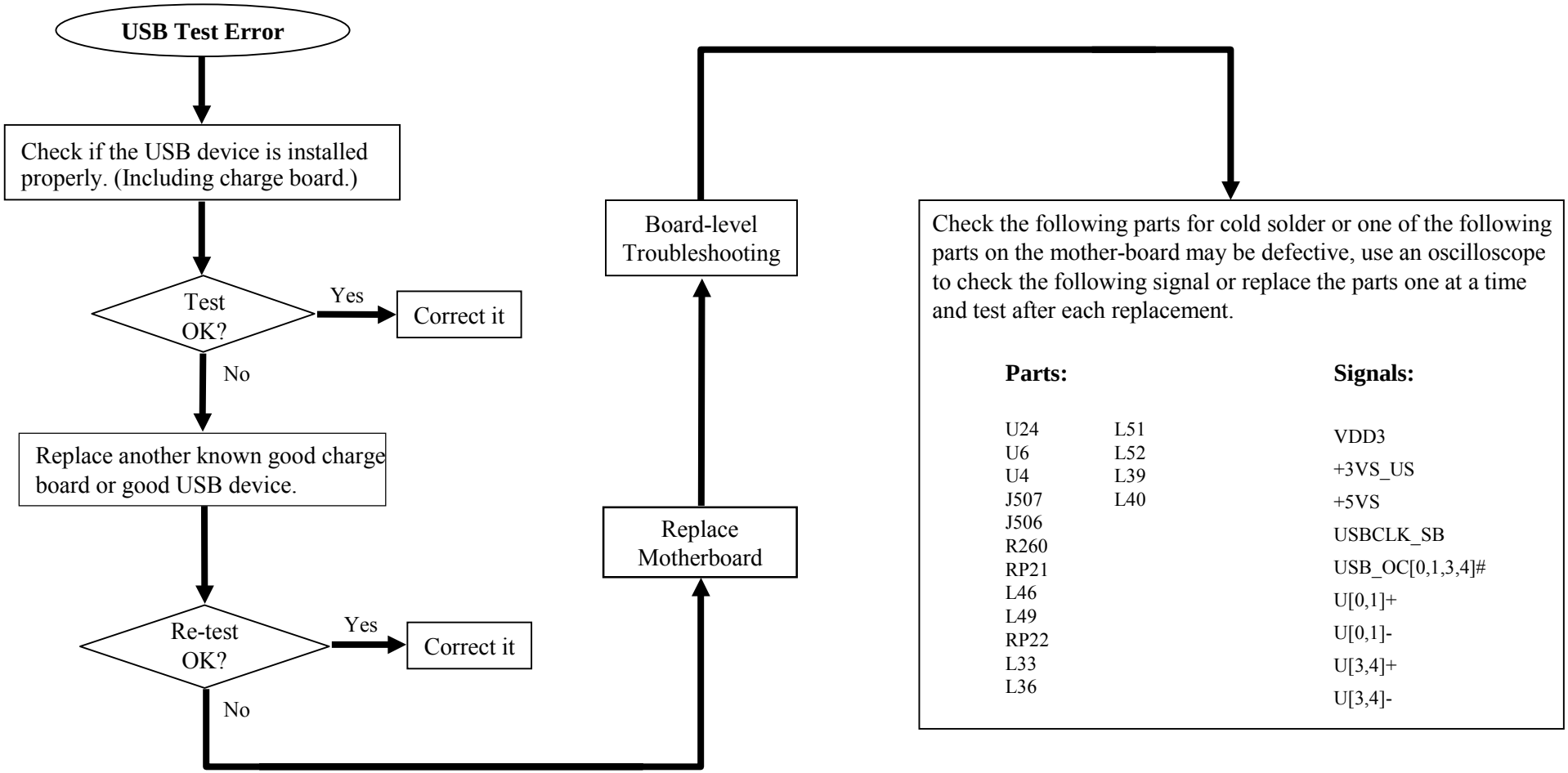
8.9 Floppy Drive Test Error

An error message is shown when loading data from disk to system.



8.10 USB Test Error

An error occurs when a USB I/O device is installed.



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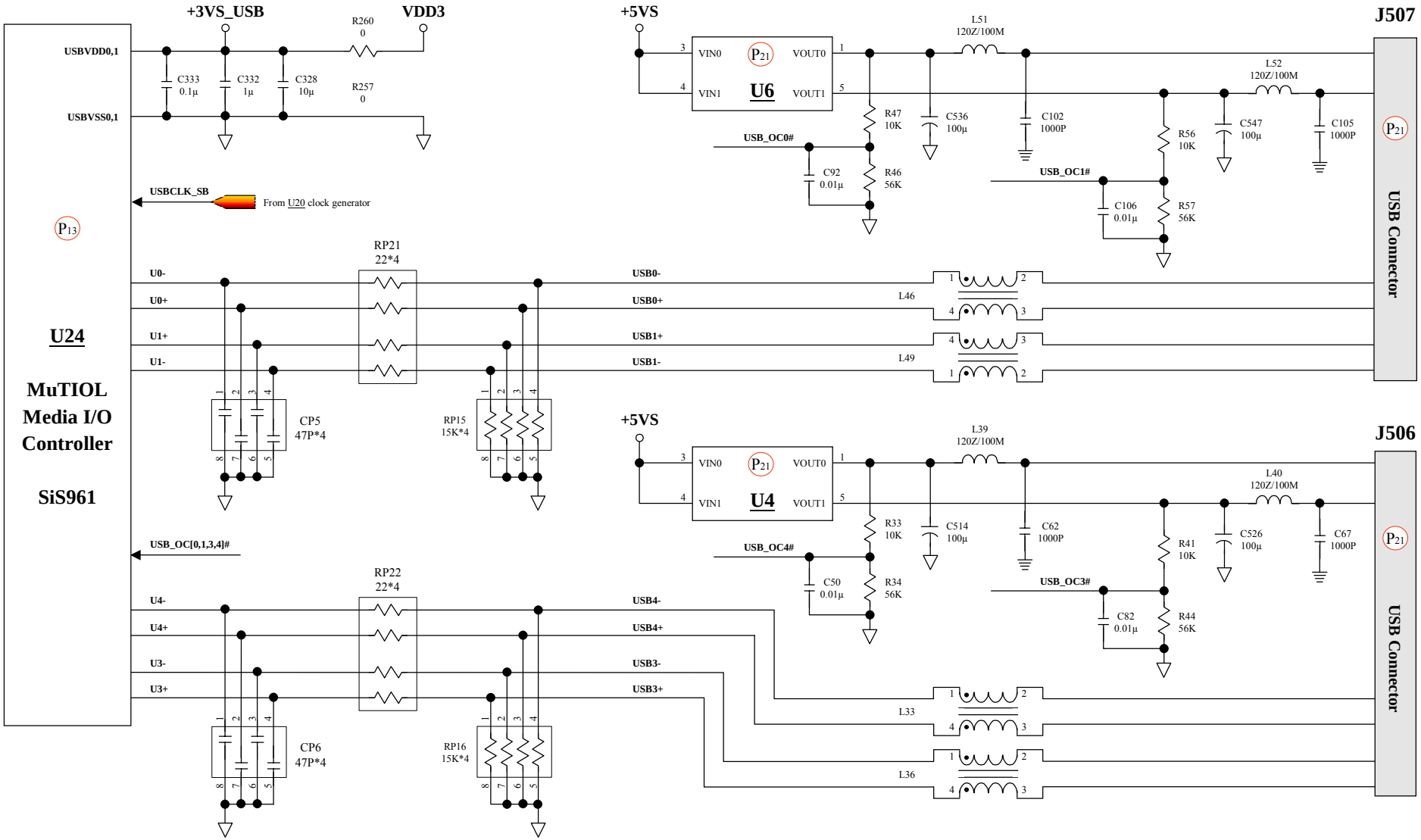
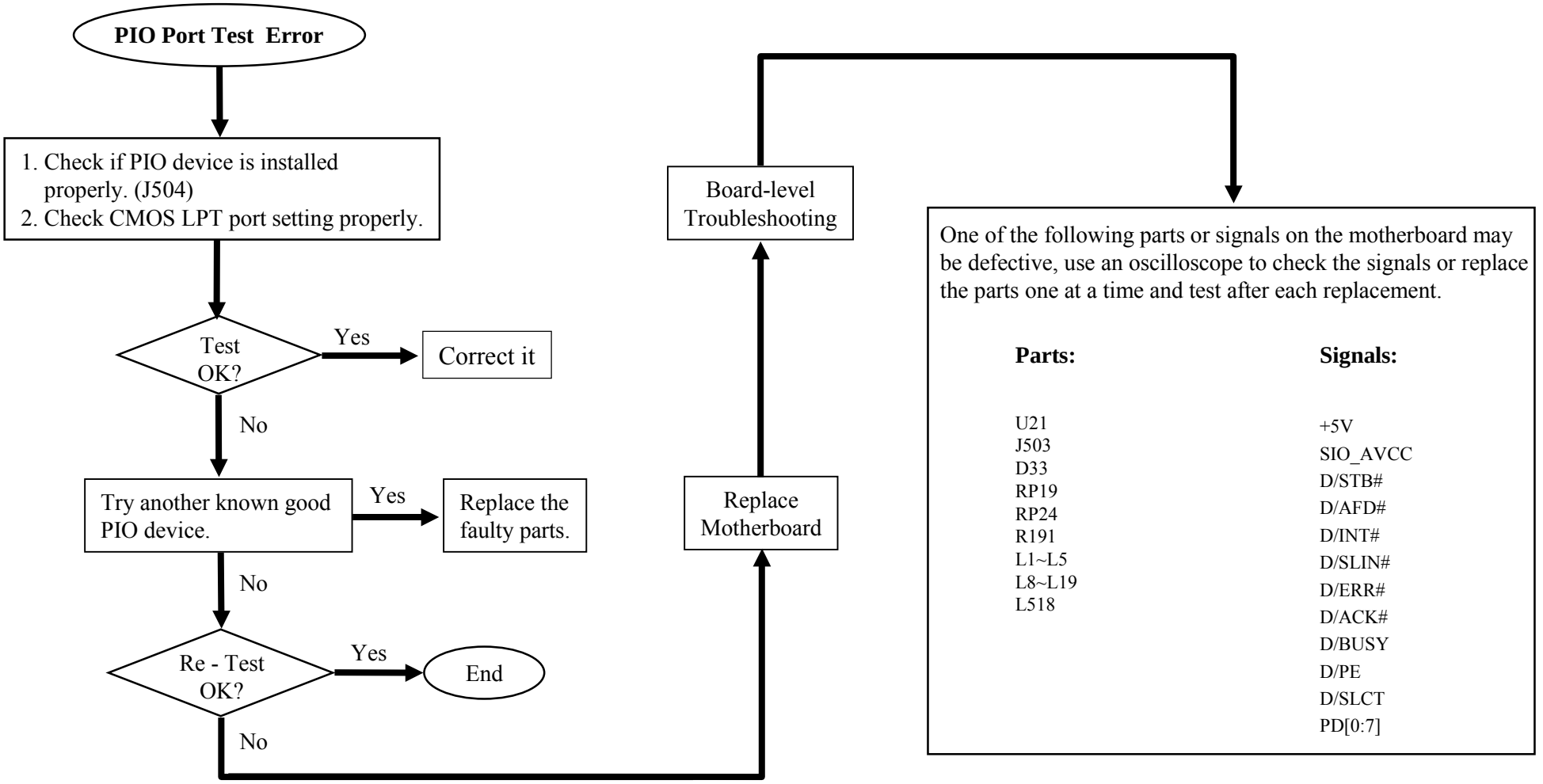
8.10 USB Test Error

An error occurs when a USB I/O device is installed.



8.11 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



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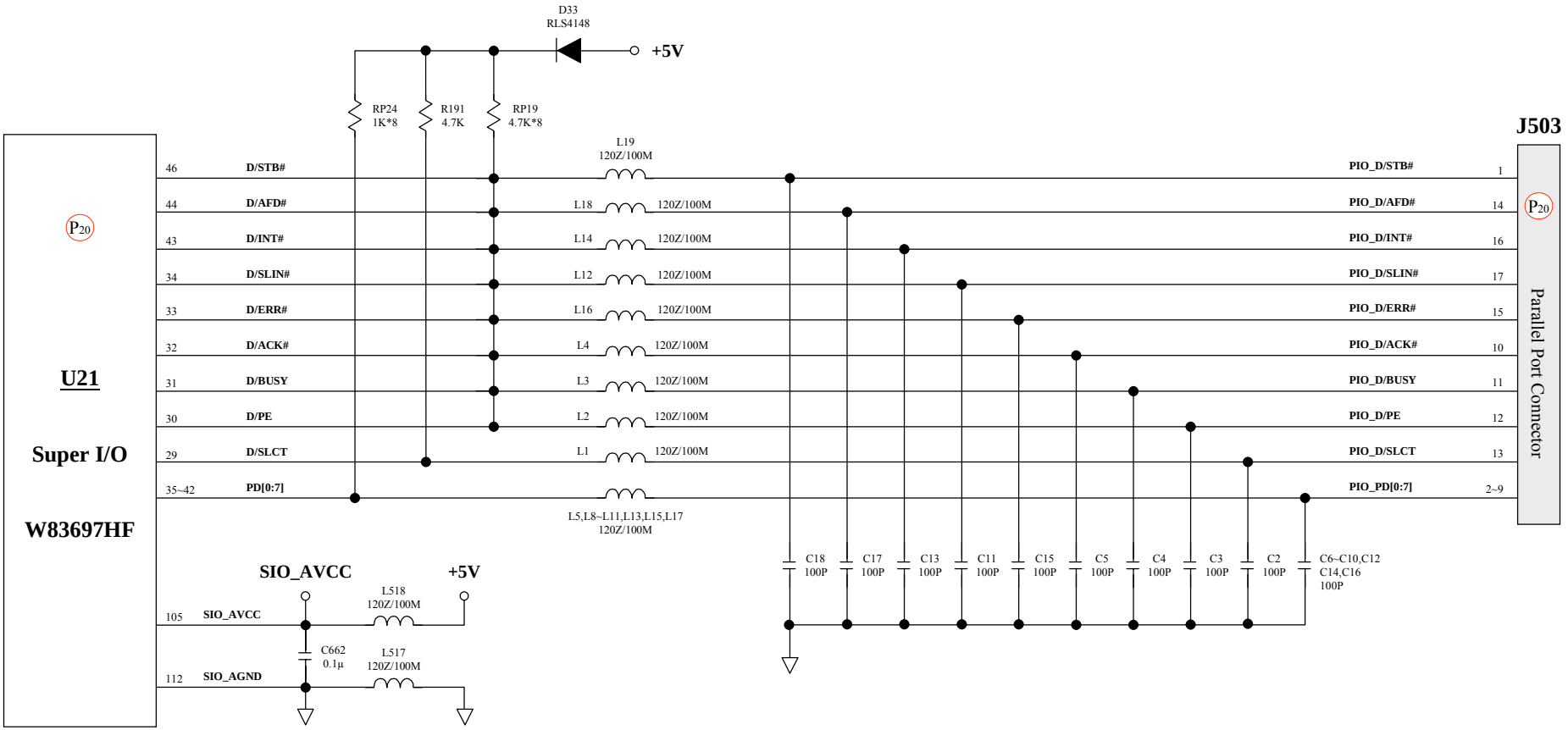
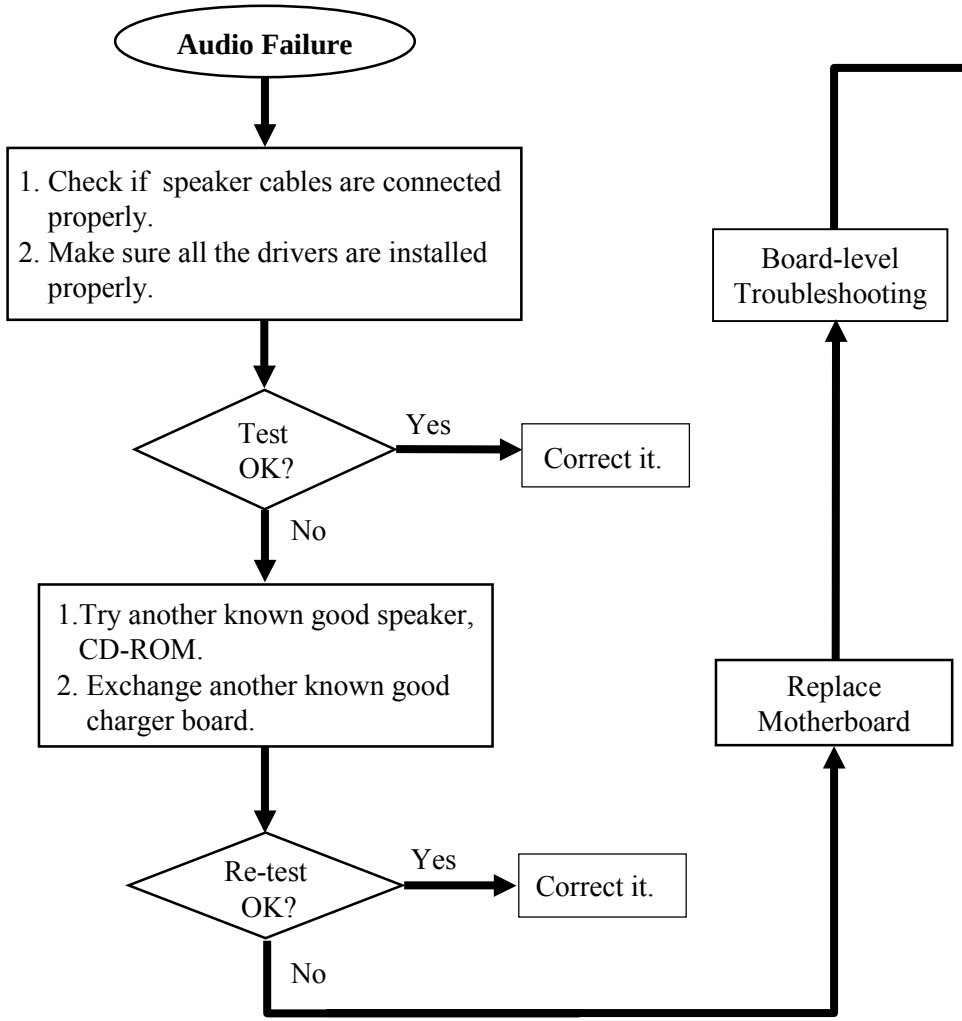
8.11 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



8.12 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U24	AOUT_R
U32	AOUT_L
U31	+3V
J31	VA
L88	SPK_OFF
L82	SPDIFOUT
L85	
Q26	
Q29	
Q28	
L84	
L97	
L526	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U24	+5V
U32	VA
J19	MIC_VREF
J32	
R627	
VDD5	
R196	
R340	
L83	
L503	
L31	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U24	CDROM_LEFT
U32	CDROM_RIGHT
J510	CDROM_COMM
R197	
R229	
R201	

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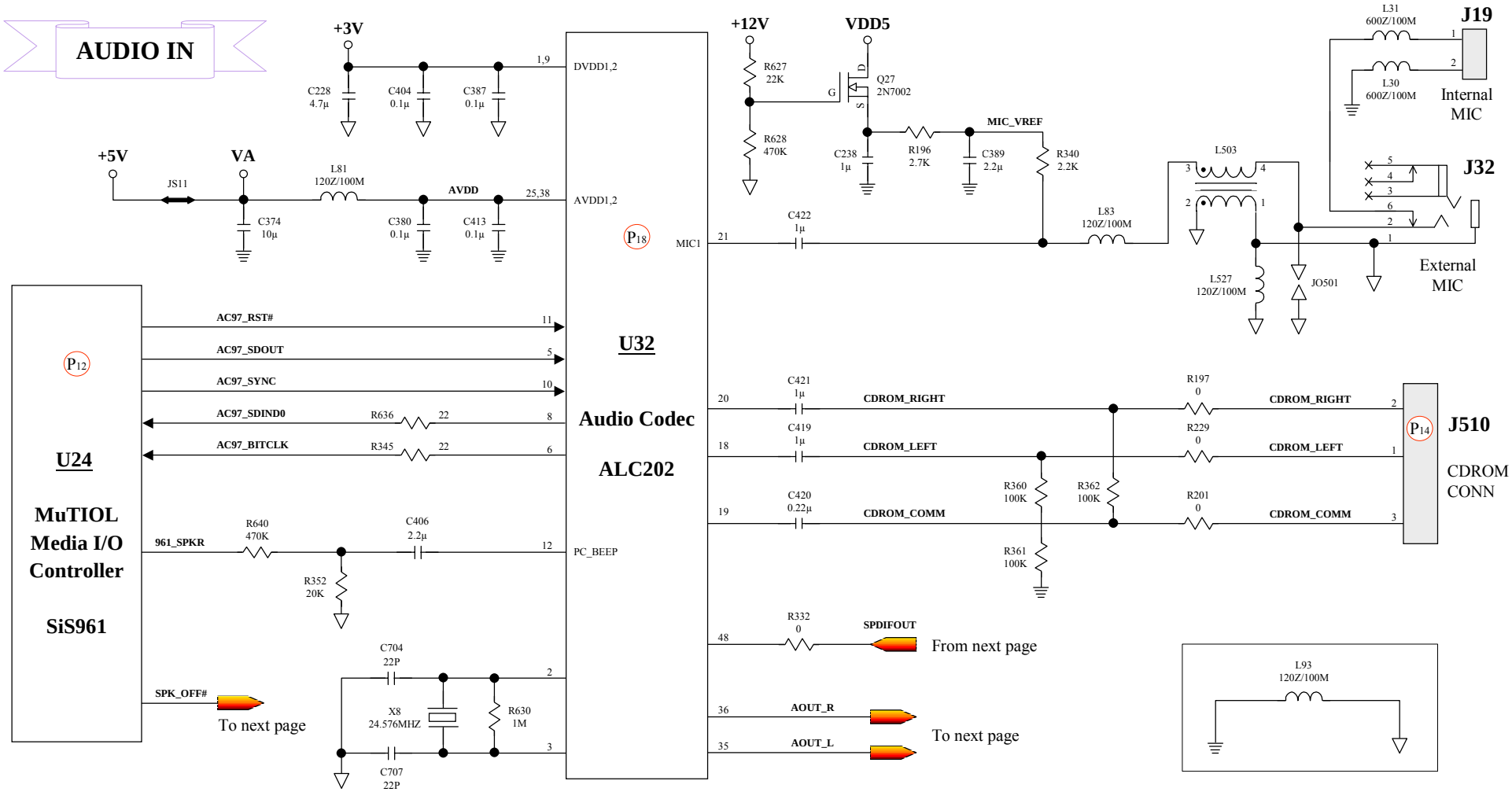
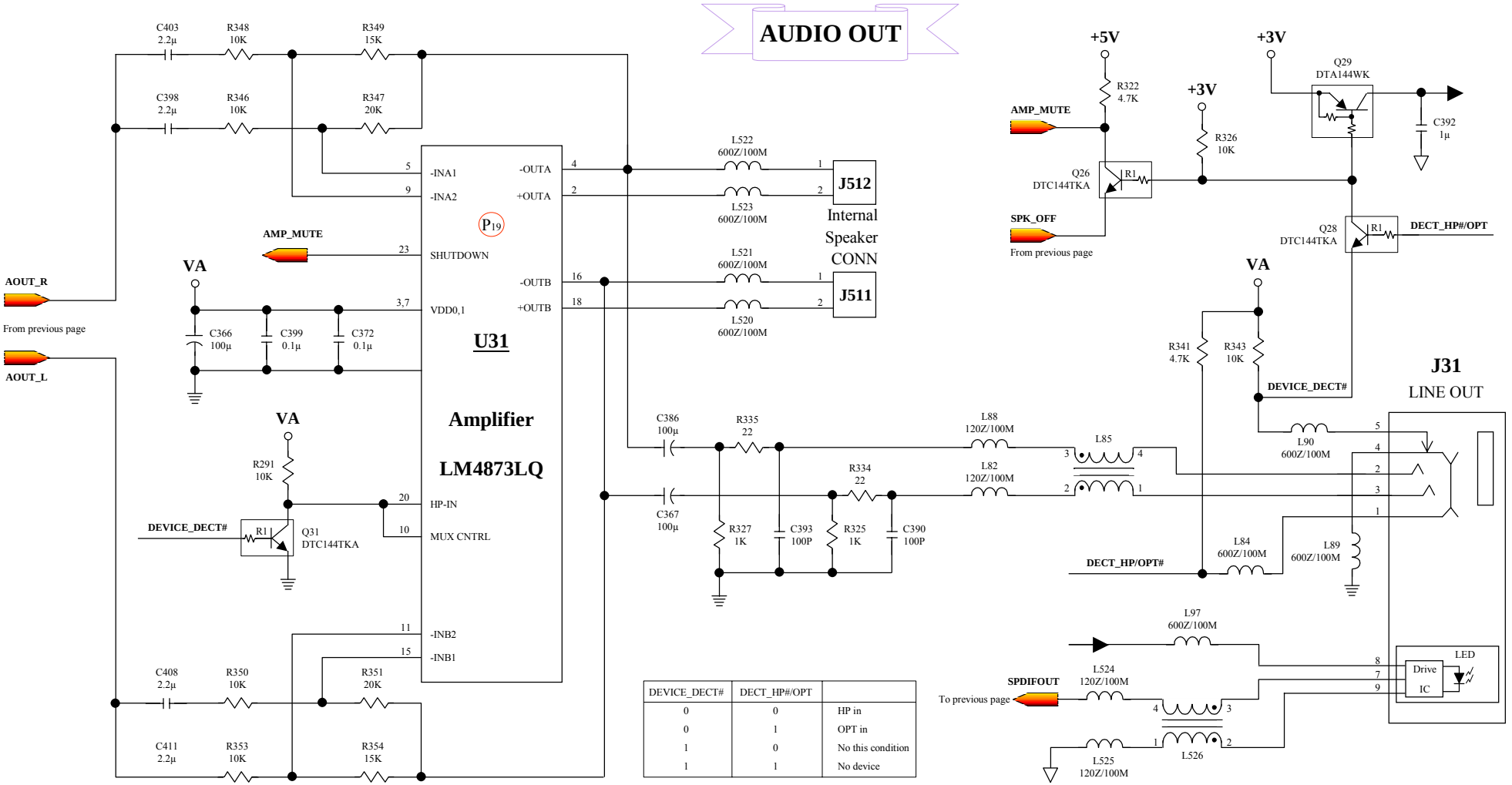
8.12 Audio Failure

No sound from speaker after audio driver is installed.



8.12 Audio Failure

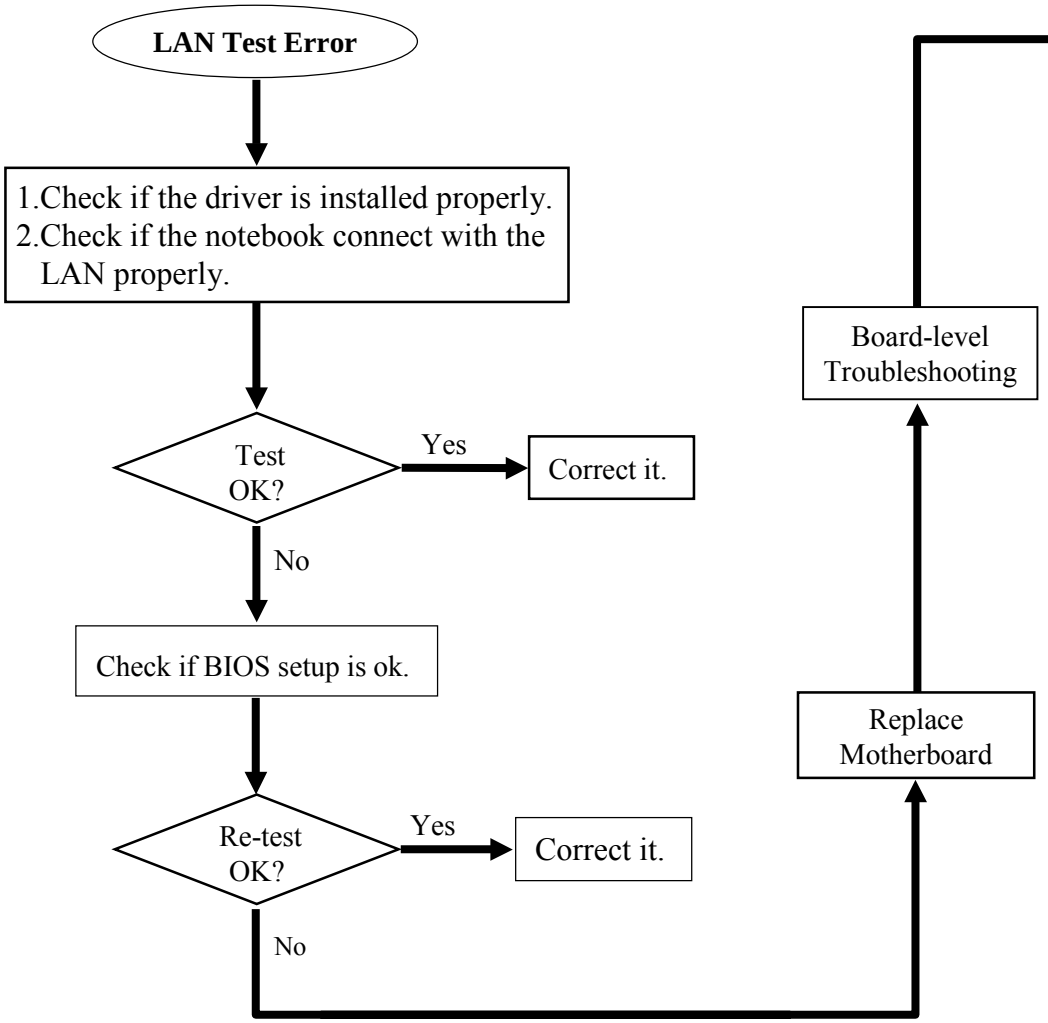
No sound from speaker after audio driver is installed.



DEVICE_DECT#	DECT_HP#/OPT	
0	0	HP in
0	1	OPT in
1	0	No this condition
1	1	No device

8.13 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U24	R559
U7	R566
U503	R565
J508	R70
R265	R553
R295	R61
R293	R62
RP35	R63
R76	R64
R83	F501
R94	U509
RP3	U510
RP2	
R626	
R388	
R713	
OSC1	

Signals:

MIIAVDD	LAN_RXN
+3VS_LAN	LAN_RXP
LAN_DATAIO	LAN_CT
LAN_DCLK	LAN_TXP
LAN_MTXD[0:3]	LAN_TXN
LAN_MTXE	PJRX+
LAN_MTXC	PJRX-
LAN_COL	PJTX+
LAN_CRS	PJTX-
LAN_MRXDV	PJ7
LAN_MRXER	PJ4
LAN_MRXC	
LAN_MRXD[0:3]	
CLK25M	

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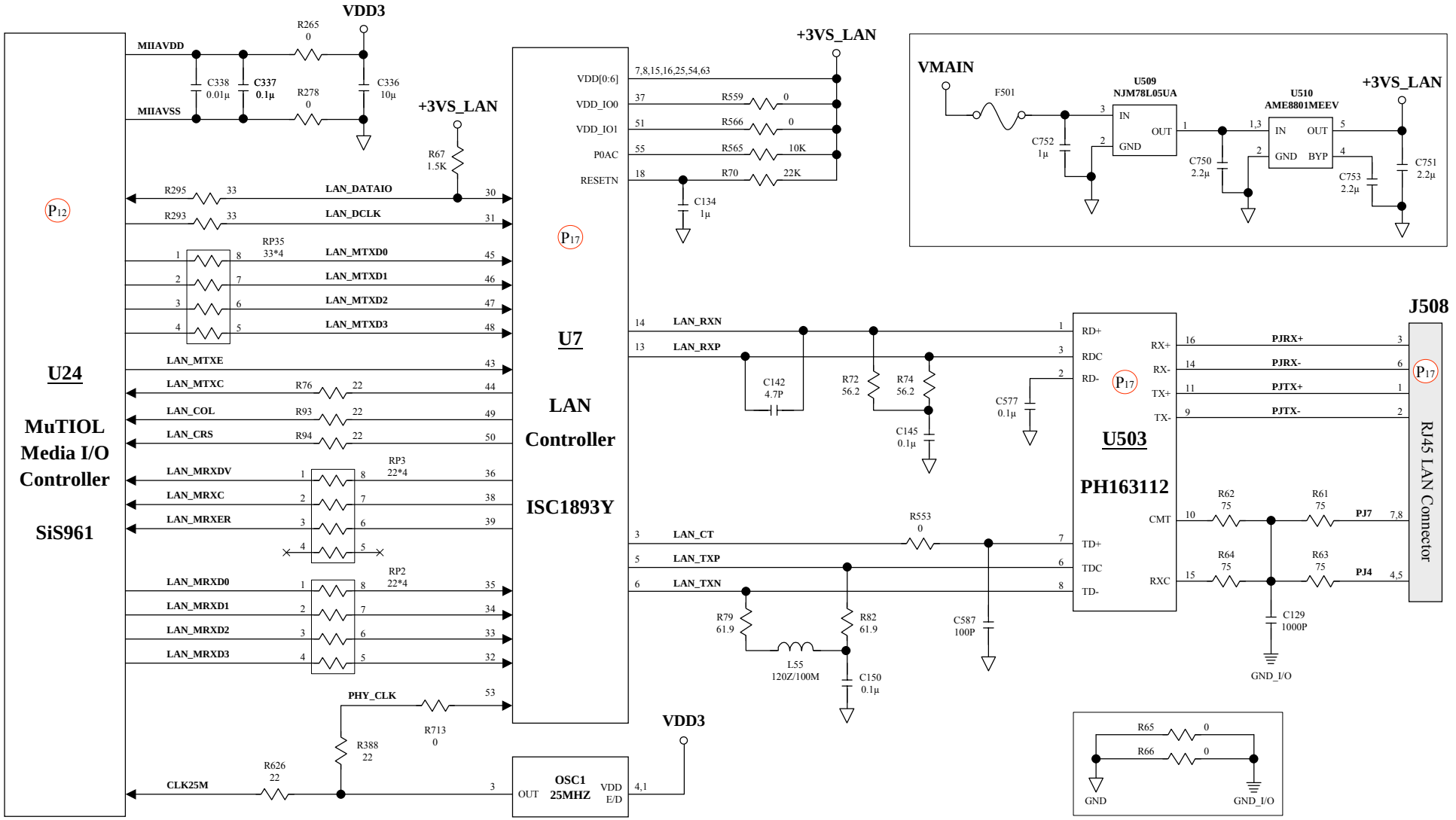
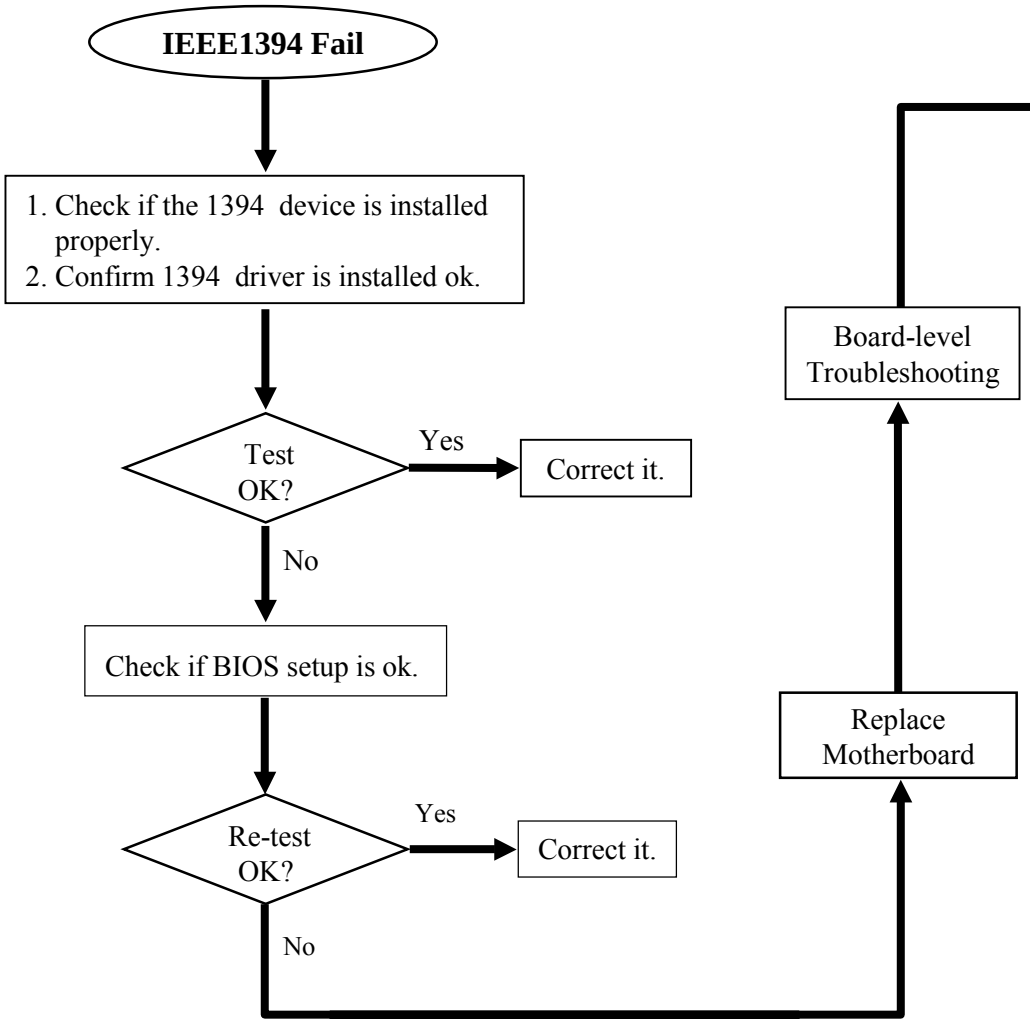
8.13 LAN Test Error

An error occurs when a LAN device is installed.



8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U24	PCI_AD[0:31]	PCI_SERR#
U25	PCI_C/BE# [0:3]	1394_PME#
U18	PCI_REQ1#	PCI_1394_CLK
J26	PCI_FRAME#	SEECS
R392	PCI_IRDY#	SEECLK
L98	PCI_TRDY#	SEEDI
L99	PCI_DEVSEL#	SEEDO
R292	PCI_STOP#	TPA+
R308	PCI_IRQC_1394#	TPA-
R301	PCI_RESET#	TPB+
R312	PCI_GNT1#	TPB-
R381	PCI_PAR	TPBIAS1
R382	PCI_PERR#	+3V
R383		+3V_1394
R384		PHYVDD
X1		

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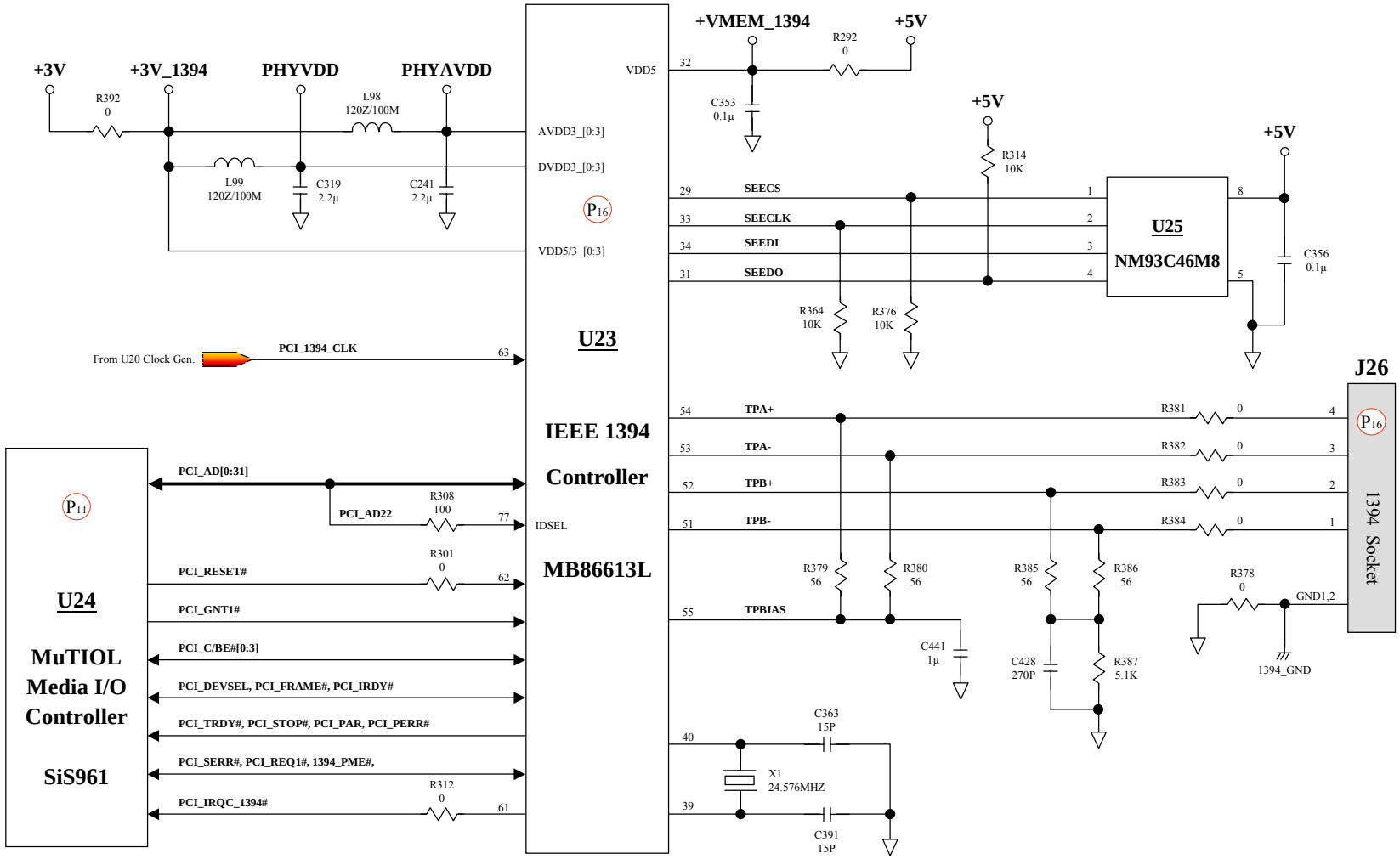
8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



9. Spare Parts List - 1

Part Number	Description	Location(s)
442672200001	AC ADPT ASSY;19V,4.74A,DELTA,850	
541667220030	AK;28-PR,BOX,8500	
346600000534	AL-FOIL/MYLAR;T=0.1,W=100,PRC	
346672200012	AL-FOIL;M/B-COMPONENT SIDE-1,850	
346672200011	AL-FOIL;M/B-SOLDER SIDE-1,8500	
298000000005	BATTERY HOLDER;EC-3211-4,SMT	BT501
338530010005	BATTERY;LI,3V/220MAH,CR2032	
242670800113	BFM-WORLD MARK;WINXP,7521N	
221671640001	BOX;AK,8175	
340672200010	BRACKET ASSY;HDD,8500	
342672200010	BRACKET;CD-ROM,8500	
342672200005	BRACKET;HDD,8500	
342672200007	BRACKET;IO,8500	
342672200001	BRKT;LCD-141,L,8500	
342672200002	BRKT;LCD-141,R,8500	
344672200014	BUTTON; TP,8500	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
332300000115	CABLE;FFC,FDD,6020	
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C16,C8
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C106,C125,C141,C144,C166,
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C7
272073104501	CAP;.1U ,25V,+80-20%,0603,Y5V,S	C1,C10,C4
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C101,C103,C110,C112,C114,
272005104502	CAP;.1U ,CR,50V,20%,0805,Z5U,SM	C602
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C32,C406,C420

Part Number	Description	Location(s)
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C376
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C102,C105,C115,C162,C214,
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C129,C557,C567
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C1,C19,C20,C25,C26,C283,C
272075101302	CAP;100P ,CR,50V,5%,0603,NPO,SMT	C100,C747,EC1,EC2,EC3,EC
272431107509	CAP;100U,2V,20%,7343,SDK-CAP	PC25,PC26
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C329,C330,C390,C393
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C137,C147,C171,C172,C173,
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	PC2,PC41,PC49,PC511,PC51
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC10,PC13,PC19,PC21,PC27
272073152401	CAP;1500P,CR,25V ,10%,0603,X7R,S	PC516
272075150701	CAP;15P ,50V ,+ -10%,0603,NPO,S	C369
272075150301	CAP;15P ,CR,50V ,5% ,0603,NPO,S	C363,C391
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C13,C3,C6
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C121,C134,C135,C152,C156,
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC5,PC502
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	C108,C113,C323,C60,C606,C
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C111,C241,C319,C322,C335,
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C5
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C711
272075200302	CAP;20P ,CR,50V ,5% ,0603,NPO,S	C370
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C741
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C10,C11,C12,C13,C14,C15,C
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C11
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C704,C707

9. Spare Parts List - 2

Part Number	Description	Location(s)
272011226703	CAP;22U,10V,+80%-20%,1206,Y5V,SM	C361,C66,C709,C87
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C428
272073332401	CAP;3300P,CR,25V ,10%,0603,X7R,S	C342,C395
272075330302	CAP;33P ,50V,5% ,0603,NPO,SMT	C23,C24,PC514
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C631
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C14,C9
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C228,C431
272072471301	CAP;470P ,CR,16V ,5% ,0603,NPO,P	C12
272075470302	CAP;47P ,CR,50V ,5%,0603,NPO,SM	C437
272431476502	CAP;47U ,6.3V,20%,SP-CON,7343,S	C2
272431476502	CAP;47U ,6.3V,20%,SP-CON,7343,S	PC557
272075509801	CAP;5P ,CR,50V,+ -.5PF,0603,NP	C142
312230680042	CAP;68P ,CR,3KV,10%,RA,PITCH7.5	
221600020128	CARTON;380MM*320MM*320MM,BC FLUT	
221671220002	CARTON;NON-BRAND,MSL,8170	
431672200001	CASE KIT;8500	
451672200091	CD ROM ME KIT;8500	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,N	
313000020379	CHOKE COIL;0.75UH,+30-10%,4.5Ts,	PL506,PL507,PL508
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L33,L36,L46,L49,L503,L526,
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	L501
313000020194	CHOKE COIL;8uH,12.5TS,D.8,55130,	PL510,PL512
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J502
331720025005	CON;D,FM,25P,2.775,R/A	J503

Part Number	Description	Location(s)
291000141203	CON;FPC/FFC,12P,0.5MM,H=6.5,ST,S	J514
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J24
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J25
291000142609	CON;FPC/FFC,26P,1MM,H=7.7,ST,SMT	J509
291000014409	CON;HDR,FM,22P*2,2.0MM,SMT,SPEED	J513
291000013016	CON;HDR,MA,15P*2,1MM,H4.25,ST,SM	J18
291000025018	CON;HDR,MA,25P*2,0.8MM,R/A,L/P,S	J510
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J21
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J19,J511,J512
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S	J504,J505
291000010614	CON;HDR,MA,6P*1,1.25MM,H4.2,ST,S	J20
291000020601	CON;HDR,MA,6P*1,1.25MM,R/A,SMT	J1
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J26
291000811002	CON;PHONE JACK,10P,RJ45,RJ11,P33	J508
291000910403	CON;POWER JACK,4P,D=13.0,SG	PJ501
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J31
291000920602	CON;STEREO JACK,6P,W9.5,RC64-06G	J32
291000920401	CON;TV/S-JACK,FM,4P,35146S-04T1-	J501
291000720803	CON;USB,DUAL PORT,FM,H15.64,R/A,	J506,J507
346600000040	CONDUCTIVE TAPE;10MM,UCTP,PRC	
346600000040	CONDUCTIVE TAPE;10MM,UCTP,PRC	
346600000040	CONDUCTIVE TAPE;10MM,UCTP,PRC	
346600000060	CONDUCTIVE TAPE;25MM,UCTP,PRC	
346600000039	CONDUCTIVE TAPE;5MM,UCTP/8269H,P	

9. Spare Parts List - 3

Part Number	Description	Location(s)
225670400006	CONDUCTIVE TAPE;LCD CABLE,GRAMPU	
225672200001	CONDUCTIVE TAPE;M/B-1,8500	
225672200001	CONDUCTIVE TAPE;M/B-1,8500	
332160000048	COPPER WIRE;2UEW,D=0.8MM,GLD,130	
313000150093	CORE;LAN CORE,230OHM/100MHZ,LF-1	
340672200016	COVER ASSY;KB,8500	
340672200001	COVER ASSY;LCD-141,8500	
340672200015	COVER ASSY;TOP,8500	
344672200013	COVER; HINGE,8500	
344672200011	COVER;HDD,8500	
344672200010	COVER;HEAT-SINK,8500	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP2,CP3
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP5,CP6
346600000142	DIALAMY;T=0.1,W=113,WHITE,PRC	
331660020003	DIMM SOCKET;DDR SODIMM 200P,AMP1	J22
331660020002	DIMM SOCKET;DDR SODIMM200P,AMP13	J23
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD2,PD3
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D2
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D25,D30,D35
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D7
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD503,PD505,PD507,PD509
288100051002	DIODE;RB051L-40,.45V,3.0A,SMT	PD502,PD504,PD506,PD508
288100751001	DIODE;RB751V-40,40V,200mA,SOD-32	Q1
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D28,D29,D3,D31,D33,D36,D

Part Number	Description	Location(s)
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD4
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C366,C367,C386,C514,C526,
312371507102	EC;1500U,6.3V, 10*12.5,.026ohm,	PC510,PC522,PC528,PC534
312272263511	EC;22U,25V,20%,RA,8*10.5,105 ,O	PC505,PC508,PC520,PC523,
312276806156	EC;680U,6.3V,+-20%,D10X12.5,6PS6	PC560
312278206155	EC;820U,4V,+-20%,D10X12.5,4PS820	PC504,PC517,PC524,PC530,
227672200001	END CAP;8500	
227672200006	END CAP;AK BOX,8500	
227670000002	END CAP;MANUAL,7521	
481672200001	F/W ASSY;SYS/VGA BIOS,8500	J29
523411442517	FD DRIVER;1.44M,3.5",D353G R69-2	
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L29,L39,L40,L41,L42,L43,L5
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L1,L10,L11,L12,L13,L14,L15
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L30,L31,L520,L521,L522,L52
273000130037	FERRITE CHIP;60OHM/100M,1608,MAG	L93
422672200002	FFC;TOUCH-PAD,8500	
342672400007	FINGER;EMI GROUNDING SMD FINGER	ETP15,ETP16,ETP18,ETP2,I
341672200001	FLAT SPRING;EMI,HDD,8500	
341672200004	FLAT SPRING;EMI,HEATSINK,8500	
341672200004	FLAT SPRING;EMI,HEATSINK,8500	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F5
295000010105	FUSE;1A,NORMAL,1206,SMT	F501,F6,F7
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF501
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	F2
295000010110	FUSE;NORMAL,2.5A/63VDC,3216,SMT	F1

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Part Number	Description	Location(s)
345672200011	GASKET;M/B-1,8500	
345672200016	GASKET;M/B-2,8500	
345672200022	GASKET;M/B-3,8500	
230000010004	GLUE;9001B,BLACK,PRC	
230000010003	GULE;9001A,BLACK,PRC	
451672200051	HDD ME KIT;8500	
343672200001	HEAT SINK;NORTHBRIDGE,8500	
340672200029	HEAT_SINK MODULE ASSY;8500	
340672200005	HINGE;L-141,8500	
340672200006	HINGE;R-141,8500	
340672200011	HOUSING ASSY;CASE,8500	
340672200002	HOUSING ASSY;LCD-141,8500	
451672200001	HOUSING KIT;8500	
344600000424	HOUSING;HIROSE/DF13-6S-1.25C,PRC	
344600000577	HOUSING;JAE/F1-S20S,PRC	
344600000701	HOUSING;JST/SHDR-30V-S-B,PRC	
344600000902	HOUSING;JWT/A1251H02-2P,PRC	
344600000903	HOUSING;JWT/A1251H02-6P,PRC	
291000614784	IC SOCKET;BGA-PGA478B-SKT,478P,M	U502
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U18
286303416001	IC;ADP3416JR,PWM DRIVER,SO8	PU502,PU504,PU505
284500201002	IC;ALC201,AC97 CODEC,TQFP,48P	U32
286305151002	IC;APL5151,LINEAR REGULATOR,1.8V	U22
286305151003	IC;APL5151,LINEAR REGULATOR,3.3V	U11,U510
284502841001	IC;CM2841,300MA CMOS LDO,SOT23-5	U3

Part Number	Description	Location(s)
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U25
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF	
286306301003	IC;HIP6301CB,PWM CTRL,SOIC,20P	PU503
284508268001	IC;HT82K68E,KBC,SSOP48,SMT	U16
284501893001	IC;ICS-1893,LAN-PHY,TQFP,64P,SMT	U7
284593722001	IC;ICS93722,DDR ZERO DELAY CLOCK	U8
284595200101	IC;ICS952001,TIMING CTL HUB FOR	U20
286100358004	IC;LM358,DUAL OP/AMP,SO,8P,TI,PR	u3
286104873001	IC;LM4873LQ,AUDIO AMPLIFIER,2.1W	U31
286100358001	IC;LMV358M,DUAL AMP.,LOW VOLT.,S	U5
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU501,PU511
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU1
286301714001	IC;MAX1714A,PWM CTLR,0SOP,20P	PU508
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU510
286300809009	IC;MAX809STR,RESET CIRCUIT,2.93V	U30
284586613003	IC;MB86613S;IEEE1394;LQFP100P,1P	U23
286307805010	IC;NJM78L05UA,VOL REGULATOR,SOT,	U10,U27,U509
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
286309173005	IC;RT9173A,3A BUS TERMINATION RE	PU509
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U4,U6
286300431010	IC;SC431CSK-1,1%,2.5V,ADJ REG,SO	PQ501
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ1
284500301004	IC;SIS301LV,TV ENCODER/LVDS,128P	U17
284500650002	IC;SIS650,N.B.,BGA702	U504
284500961003	IC;SIS961 HM-I/O,S.B.,BGA371	U24

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Part Number	Description	Location(s)
284583697004	IC;W83697HF,SI/O,PQFP,128P,SMT	U21
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PL511
273000150106	INDUCTOR;4.7UH,10%,2012,30mA,SMT	L38,L44
346672200003	INSULATOR;HDD,8500	
346669600014	INSULATOR;INVERTER,REDSEA	
346672200004	INSULATOR;M/B-DDR,8500	
346672200002	INSULATOR;PLATE-KB,8500	
541150310001	INVERTER BD;7521	
531099990204	KBD OPTION;88,UI,8500	
531017240055	KBD;88,KS-26IA-UILG01,ZIPPY,8500	
451672200071	LABEL KIT;NON-BRAND,8500	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000457	LABEL;20*7MM,COMMON,PRC	
242662300009	LABEL;25*10MM,3020F	
624200010140	LABEL;5*20,BLANK,COMMON	
242672200002	LABEL;AGENCY-GLOBAL,MSL,8500	
242600000157	LABEL;BAR CODE & S/N,13.5*75,COM	
242669900009	LABEL;BLANK,60*80MM,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000446	LABEL;S/N,INVERTER,20MM*3MM,PRC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441672200002	LCD ASSY;QDI,14",8500	
451672200032	LCD ME KIT;QDI,14",8500	
413000020322	LCD;QD141X1LH03,TFT,14",LCDS,XGA	

Part Number	Description	Location(s)
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D43,D44,D45,D46,D47,D48,
526267220021	LTXNX;8500/T4XX/XXB/7UI7/L2D3AXL	
561567220011	MANUAL KIT;PR,8500,N-B	
561567220023	MANUAL;USER'S,PR,8500,N-B	
421672200007	MICROPHONE ASSY;LCD,8500	
339115000035	MICROPHONE;PVM-6BU-1,PRC	
313000150244	MPP CORE;55130,OD=11.9,ID=5.89,H	
346600000074	MYLAR;T=0.1,W=110,BLACK,PRC	
416267220901	NB PF OPTION;XGA,14.1",8500	
416267220002	NB PF;QDI,14",8500	
375102030010	NUT-HEX;M2,2,NIW	
274042500405	OSC;25MHZ,50PPM,3.3V,15PF,H=1,SM	OSC1
461672200001	PACKING KIT;NON-BRAND,8500	
221672250003	PARTITION;AK BOX,8500	
221600050113	PARTITION;FLAT,320MM*290MM,BC FL	
412600000028	PCB ASSY;MDC,56K,V1456VQL-P1,ASK	
316503100003	PCB;PWA-7521/INVERTER BD	
316672200001	PCB;PWA-8500/MOTHER BD	R02
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222667220003	PE BAG;L560XW345,CERES	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100	L505,L506,L507,L508,L509,L
340672200017	PLATE ASSY;KEYBOARD,8500	
342672200008	PLATE;KEYBOARD,8500	
411503100004	PWA;PWA-7521/INVERTER BD	
411503100005	PWA;PWA-7521/INVERTER BD,SMT	

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Part Number	Description	Location(s)
411670800013	PWA;PWA-7521N,INVERTER BD,OZ965,	
411672200001	PWA;PWA-8500,MOTHER BD	
411672200003	PWA;PWA-8500,MOTHER BD,SMT	
411672200002	PWA;PWA-8500,MOTHER BD,T/U	
332810000102	PWR CORD;250V10A,2P,BLK,CHINA,15	
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR538
271125017101	RES;.01,1W,1%,3720,SMT	PR523,PR534
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R168,R245,R246,R257,R265,
627107100001	RES;0 ,1/16W,0603,SMT	R20
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR19,PR3,PR4,PR512,PR513
271071132101	RES;1.3K ,1/16W,1% ,0603,SMT	R5
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R528,R557
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R67
271002100301	RES;10 ,1/10W,5% ,0805,SMT	R32
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR545,R100,R103,R112,R11
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R35,R43
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R111,R115,R193,R308
271071104701	RES;100K ,1/16W,.1%,0603,SMT	PR503,PR535,R2
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R10,R16,R8
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR1,PR18,PR501,PR508,R3,
271071103701	RES;10K ,1/16W,.1%,0603,SMT	PR13,PR527,PR529
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR11,PR2,PR502,PR516,PR5
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R302
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R90
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R558

Part Number	Description	Location(s)
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R104
271071137311	RES;137K ,1/16W,1% ,0603,SMT	PR507
271071147011	RES;147 ,1/16W,1% ,0603,SMT	R144
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R101,R192,R202,R369,R509,
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R1
271071154101	RES;150K ,1/16W,1% ,0603,SMT	PR16
271071158311	RES;158K ,1/16W,1% ,0603,SMT	PR20
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R349,R354
271071163101	RES;16K ,1/16W,1% ,0603,SMT	R1
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R550,R551
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R198,R199,R20,R21,R25,R28
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R11
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR21,R55
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R102,R107,R182,R282,R630,
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R12,R14,R340
271071261111	RES;2.61K,1/16W,1% ,0603,SMT	PR509
271002274111	RES;2.74K,1/8W ,1% ,0805,SMT	PR506,PR520,PR522
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R196
271071200101	RES;20 ,1/16W,1% ,0603,SMT	PR528,R97
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R583
271071205311	RES;205K ,1/16W,1% ,0603,SMT	R50
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R347,R351,R352
271071215211	RES;21.5K,1/16W,1% ,0603,SMT	PR14
271071220101	RES;22 ,1/16W,1% ,0603,SMT	R9
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R108,R117,R170,R174,R175,

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Part Number	Description	Location(s)
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R367,R368
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R627,R70
271071237211	RES;23.7K,1/16W,1% ,0603,SMT	PR504
271071243211	RES;24.3K,1/16W,1% ,0603,SMT	R2
271071241301	RES;240 ,1/16W,5% ,0603,SMT	R365,R366
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R521
271071271101	RES;270 ,1/16W,1% ,0603,SMT	R14
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R142,R77
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R582
271071303101	RES;30K ,1/16W,1% ,0603,SMT	R4
271071303301	RES;30K ,1/16W,5% ,0603,SMT	R283
271071316211	RES;31.6K,1/16W,1% ,0603,SMT	R6
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R109,R110,R15,R155,R159,R
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R516
271071391302	RES;390 ,1/16W,5% ,0603,SMT	R344
271071392311	RES;392K ,1/16W,1% ,0603,SMT	R45
627107139351	RES;39K ,1/16W,.5%,0603,SMT	R7
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	PR511
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR537,R118,R121,R143,R15
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR536,R54
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR505,PR533,R650
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R105,R18,R6,R628,R640
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R154
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R166
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R152,R153,R161,R162,R37,R

Part Number	Description	Location(s)
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	R337,R377,R387
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R164,R275
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R24,R503,R504,R505,R506,R
271071511812	RES;51.1,1/16W,1% 0603,SMT	R508,R545
271071514301	RES;510K ,1/16W,5% ,0603,SMT	R13
271071511311	RES;511K ,1/16W,1% ,0603,SMT	R52
271071513301	RES;51K ,1/16W,5% ,0603,SMT	R29,R645
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R218,R219,R26,R27,R379,R3
271071562811	RES;56.2 ,1/16W,1% ,0603,SMT	R72,R74
271071563302	RES;56K ,1/16W,5% ,0603,SMT	R148,R34,R44,R46,R57
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R147
271071681111	RES;6.81K,1/16W,1% ,0603,SMT	R3
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R584
271071619811	RES;61.9 ,1/16W,1% ,0603,SMT	R79,R82
271071619011	RES;619 ,1/16W,1% ,0603,SMT	R15
271071620102	RES;62,1/16W,1% 0603,SMT	R513,R514,R534
271071681301	RES;680 ,1/16W,5% ,0603,SMT	PR15,R370,R371,R372,R538
271071698201	RES;69.8K,1/16W,1% ,0603,SMT	R12
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R61,R62,R63,R64,R92,R98
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R532,R7,R8
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R264,R274,R398,R561
271071931211	RES;93.1K,1/16W,1% ,0603,SMT	PR17
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP12,RP14,RP18,RP53
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP518,RP520,RP522
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP507,RP509,RP510,RP512,

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Part Number	Description	Location(s)
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP4,RP41,RP501,RP9
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP43
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP15,RP16,RP17
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP13,RP535
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP24,RP502
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP2,RP21,RP22,RP3
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP35
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP503,RP504,RP505,RP506,
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP40
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP19,RP31,RP32,RP44,RP45
271621471301	RP;470*4,8P,1/16W,5%,1206,SMT	RP516
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP1
345672200001	RUBBER;LCD DOWN,8500	
345600000027	RUBBER;OD7.3*ID6,L=7mm,PRC	
565167220001	S/W;CD ROM,SYSTEM DRIVER,8500	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
340672200030	SHIELDING ASSY,TOP,8500	
342672200006	SHIELDING;FDD,8500	
333050000088	SHRINK TUBE;600V,125'C,OD=12,BLK	
333050000081	SHRINK TUBE;600V,125'C,OD2.0MM,F	
333050000098	SHRINK TUBE;ULCSA,125'C,D0.7MM,B	
333050000079	SHRINK TUBE;ULKSA,125'C,F32,OD1.	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	

Part Number	Description	Location(s)
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010702	SPC-SCREW;M2L7,K-HD,NLK,NIW	
370103010303	SPC-SCREW;M3L3,NIB,K-HD(+)	
421672200010	SPEAKER ASSY;8500	
226600030096	SPONGE;CR-4305,T=2.5,W=50,BLACK,	
345670400051	SPONGE;HOUSING-HDD,GRAMPUS	
345672200023	SPONGE;LCD BRKT-141,8500	
341670400014	SPRING;M/B SHIELD,GRAMPUS	
341672200002	SPRING-SCREW;HEAT SINK,8500	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	
295000020002	SURGE PROTECTOR;P2600SB,2P,DO-21	R60
297120100006	SW;DIP,SPST,5P,24VDC,50MA,STS-KA	SW2
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW4,SW5
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,	SW1
225600000118	TAPE;3M-467,W=16.5,PRC	
225600000089	TAPE;3M-467,W=331,PRC	
225600000361	TAPE;3M-467/DOUBLE RELEASE PAPER	
225600000029	TAPE;ACETUM ADHESIVE,W=20mm,BLK,	
225600000032	TAPE;ACETURM ADHESTIVE,W=4mm,BLK	

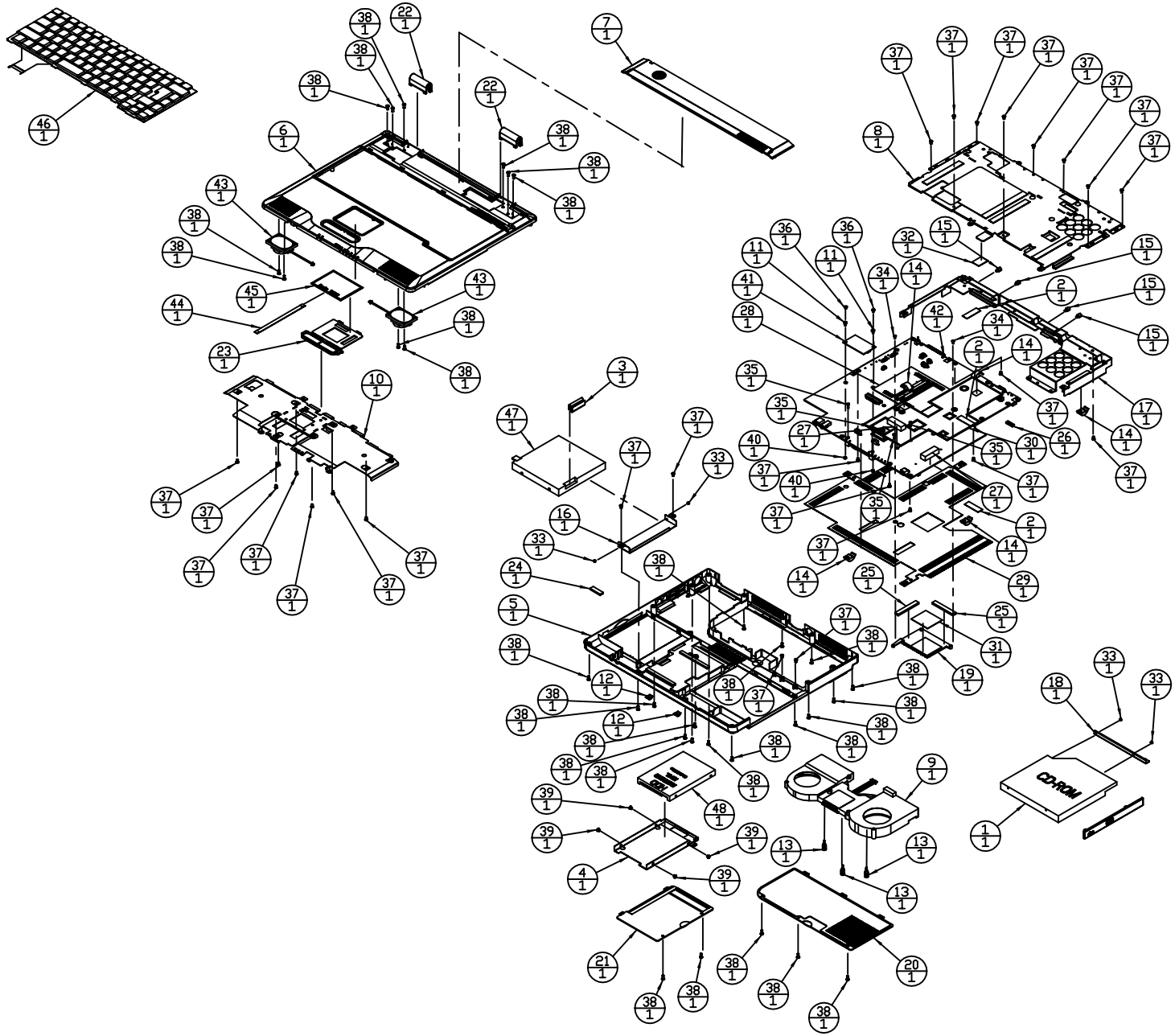
9. Spare Parts List - 9

Part Number	Description	Location(s)
225600000034	TAPE;ACETURN ADHESI,W=10mm,PRC	
225600000034	TAPE;ACETURN ADHESI,W=10mm,PRC	
225600000042	TAPE;ACETURN ADHESIVE,L566*W15,U	
225600000043	TAPE;ACETURN ADHESIVE,L84*W30,UN	
225600000110	TAPE;G9000,W=50,PRC	
225600000217	TAPE;G9000/DOUBLE RELEASE PAPER,	
333334000046	TERMINAL;HRS/DF13-2630SCF,PRC	
333334000084	TERMINAL;JAE/FI-C3-A1-15000,PRC	
333334000099	TERMINAL;JST/SSH-003T-P0.2,PRC	
333334000106	TERMINAL;JWT/A1251TOP-2,PRC	
333334000106	TERMINAL;JWT/A1251TOP-2,PRC	
346672200014	THERMAL-PAD;20*15*0.5,8500	
346672200013	THERMAL-PAD;36*32*0.5,8500	
442164900012	TOUCH PAD MODULE;TM41P-311,SYNAP	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ503,PQ515,Q14,Q27
288200144002	TRANS;DTA144WK,PNP,SMT	Q29
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q1,Q10,Q11,Q12,Q16,Q17,Q
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ512,Q15,Q20,Q30
288206035002	TRANS;FDB6035AL,30V/48A,.017OHM,	PQ502,PQ505,PQ507
288206676003	TRANS;FDB6676,30V/84A,.0075OHM,N	PQ504,PQ506,PQ509
288206690001	TRANS;FDS6690A,N-MOSFET,.017OHM,	PQ510
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q3,Q35,Q36,Q4,Q5,Q6
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q18,Q19,Q505
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q504
288214404001	trans;s14404DY,N-MOS,.008OHM,SO8	PQ514,PQ516

Part Number	Description	Location(s)
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q13,Q2,Q37
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	U2
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU2,PU506,Q8,U9
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PQ508
288204894001	TRANS;SI4894DY,N-MOSFET,018OHM,S	PQ513,PU507
273001050068	TRANSFORMER;10/100 BASE,NS601680	U503
421672200006	WIRE ASSY;INVERTER,8500	
421672200003	WIRE ASSY;LCD-141,QDI,8500	
332110028053	WIRE;#28,UL1691,GRAY,PRC	
332110030052	WIRE;#30,UL1571,OD0.6mm,BLUE,PRC	
332110030055	WIRE;#30,UL1571,OD0.6mm,GREEN,PR	
332110030053	WIRE;#30,UL1571,OD0.6mm,PURPLE,P	
332110030056	WIRE;#30,UL1571,OD0.6mm,RED,PRC	
332110030051	WIRE;#30,UL1571,OD0.6mm,WHITE,PR	
332110030054	WIRE;#30,UL1571,OD0.6mm,YELLOW,P	
332110032036	WIRE;#32,1571,BLACK/RED/#28,DRAI	
332110032002	WIRE;#32,UL1571,GRAY,PRC	
332110032003	WIRE;#32,UL1571,ORANGE/BLK,PRC	
332110032035	WIRE;#32,UL1571,RED/BLK,TWIST,A-	
332110032004	WIRE;#32,UL1571,RED/WHT,PRC	
332110032001	WIRE;#32,UL1571,WHT,PRC	
273001050047	XSFORMER;SIT16260-9.8B,16T/2600T	T1
274011431406	XTAL;14.318MHZ,30PPM,32PF,H2.5,S	X3
314100245502	XTAL;24.576MHZ,16PF,30PPM,11.5*5	X1,X8
314100327214	XTAL;32.768KHZ,12.5PF,20PPM,3*8,	X6

9. Spare Parts List - 10

Part Number	Description	Location(s)
	P/N:526267220021	



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1		CD-ROM DRIVER	1	PART	
2	225672200001	CONDUCTIVE TAPE;M/B-1,8500	3	PART	
3	332300000115	CABLE; FFC,FDD,6020	1	PART	IN
4	340672200010	BRACKET ASSY;HDD,8500	1	ASSEMBLY	
5	340672200011	HOUSING ASSY;CASE,8500	1	ASSEMBLY	
6	340672200015	COVER ASSY;TOP, 8500	1	ASSEMBLY	
7	340672200016	COVER ASSY; KB, 8500	1	ASSEMBLY	
8	340672200017	PLATE-ASSY;KEYBOARD,8500	1	ASSEMBLY	
9	340672200029	HEAT_SINK MODULE ASSY;8500	1	ASSEMBLY	
10	340672200030	SHIELDING ASSY,TOP,8500	1	ASSEMBLY	
11	341668300008	STANDOFF;MDC,MODEM,NLK,HOPE	2	PART	
12	341672200001	FLAT SPRING;EMI,HDD,8500	2	PART	
13	341672200002	SPRING-SCREW;HEAT SINK,8500	3	PART	
14	341672200004	FLAT SPRING;EMI,HEATSINK,8500	5	PART	
15	342665500008	CFM-SUYIN; S-STANDOFF	4	PART	IN
16	342672200006	SHIELDING;FDD,8500	1	PART	
17	342672200007	BRACKRT;ID,8500	1	PART	0.000
18	342672200010	BRACKET;CD-ROM,8500	1	PART	IN
19	343672200001	HEAT SINK;NORTHBRIDGE,8500	1	PART	
20	344672200010	COVER;HEAT-SINK,8500	1	PART	
21	344672200011	COVER;HDD,8500	1	PART	
22	344672200013	COVER; HINGE, 8500	2	PART	
23	344672200014	BUTTON; TP, 8500	1	PART	
24	345670400051	SPONGE,HDD,GRAMPUS	1	PART	
25	345672200011	GASKET;M/B-1,8500	2	PART	
26	345672200016	GASKET;M/B-2,8500	1	PART	
27	345672200022	GASKET;M/B-3,8500	2	PART	
28	346672200004	INSULATOR;M/B-DDR,8500	1	PART	
29	346672200011	AL-FOIL;M/B-SOLDER SIDE-1,850	1	PART	
30	346672200012	AL-FOIL;MB-COMPONENT SIDE-1,8500	1	PART	
31	346672200013	THERMAL-PAD;36*32*0.5,8500	1	PART	
32	346672200014	THERMAL-PAD;20*15*0.5,8500	1	PART	
33	370102010204	SPC-SCREW; M2L2NIW/NLK,K-HD	4	PART	IN
34	370102010407	SPC-SCREW; M2L4 K-HEAD,NIB/NLK	2	PART	IN
35	370102010702	SPC-SCREW	4	PART	IN
36	370102610302	SPC-SCREW; M2.6L3 NIB,K-HD,NYLOK	2	PART	IN
37	370102610401	SPC-SCREW; M2.6L4 K-HEAD,NIB,NLK	25	PART	IN
38	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	30	PART	IN
39	370103010303	SPC-SCREW;M3L3,NIW,K-HD(+)	4	PART	OUT
40	375102030010	NUT-HEX; M2L2,NIW	2	PART	IN
41	411669600006	PWA;PWA-RACE,MDC TRANS BD	1	PART	OUT
42	411672200001	PWA;PWA-8500,MOTHER BD	1	ASSEMBLY	0.000
43	421672200010	SPEAKER ASSY;8500	2	PART	0.000
44	422672200002	FFC;TOUCH PAD,8500	1	PART	IN
45	442164900012	TOUCH PAD;TM41P-311,SYNAPTICS	1	ASSEMBLY	
46	531020237434	KBD;88,US,K010718I1,8500	1	PART	
47		FDD DRIVER;1.44M,3.5"	1	PART	
48		HDD DRIVER	1	PART	OUT

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	21-Mar-02	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.30	DRAWING NAME	CASE KIT;8500		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD431672200001R00		

MITAC Technology Corp.

model name8500-ASSY

file name8500-EXPLODE

SHEET NO. 1 of 1

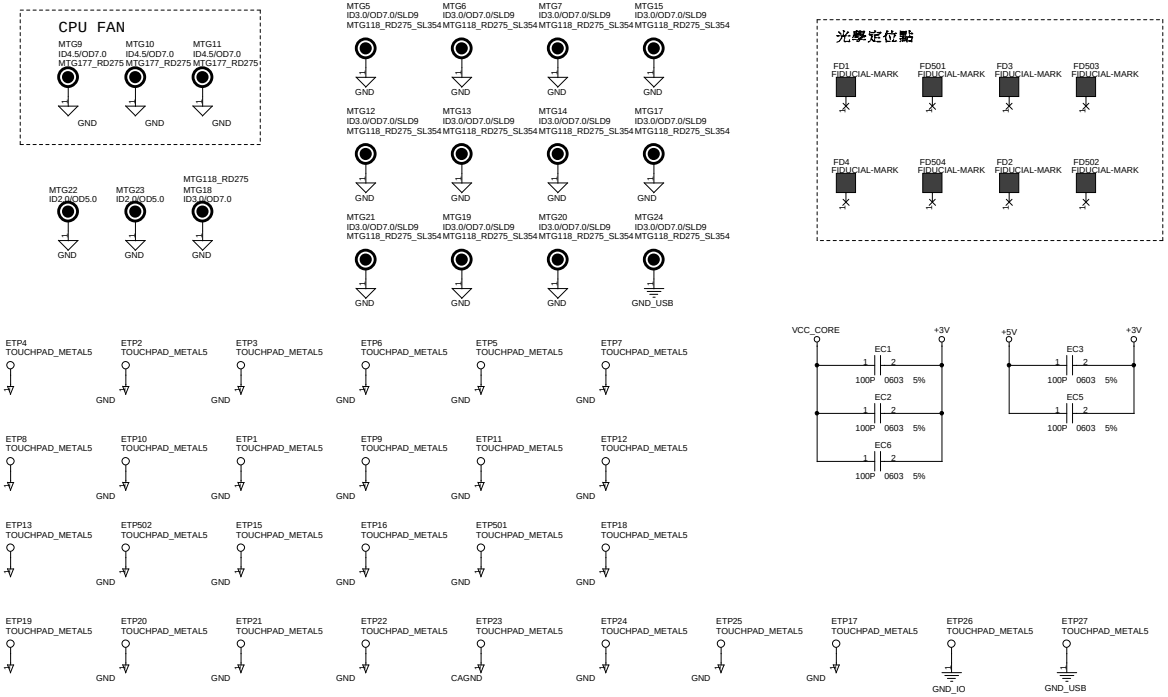
8500 R01

PROJECT CODE- G005
PRODUCT CODE- 6722

PCB P/N 316672200001
ASSY P/N 411672200001

PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
MINIPCI	PCIINTD#	REQ2#/GNT2#	AD21
IEEE1394	PCIINTC#	REQ1#/GNT1#	AD22

REVISION	TAPEOUT DAY	HISTORY
R00	2002/1/2	DESIGN FOR EVT
R0A	2002/3/11	Design for EVT2 1.Delete CARD READER function then add IEEE1394. 2.ADD deepswitch(SW501) for mobil CPU. 3.For SIS301LV, change R144 with 147, R147 to 6.04K and C315/NA . 4.Change SIS961 GPIO definitions. 5.Change KBC function from EMC to HT82K68E then Add debounce ability and hot key function on it. 6.Add powerdown function on MINI-PCI in pin98 for AMBIT and pin13 for GEMTEC. 7.Change MDC pin17 with VDD3 power plane. 8.Change SPDIFOUT function form SIS961 to ALC201. 9.Change USB connector1. 10.Change VDD5 and VDD3 power plane by LP2951 regulator, and add one VDD3 single used for LAN.
R0B	2002/4/4	Design for DVT 1. Change FAN throuth hole size. 2. Change Lan +3V_LAN regulator. 3. Add EMI solution on audio port. 4. Inverse Touchpad connector.
R0C	2002/4/10	Design for DVT The schematic is same as R0B, but it is 6-layer.
R01	2002/5/17	modify for PVT 1. add I-limit circut. 2. change VDD3 regulator to NRM78l05UA+APL5151-3.3V 3. del LAN_GND



DRAWN	DESIGN	CHECK	ISSUES

MiTAC

Title: 8500

Size: C | Document Number: PCB 316672200001/ASSY 411672200001 | Rev: R01

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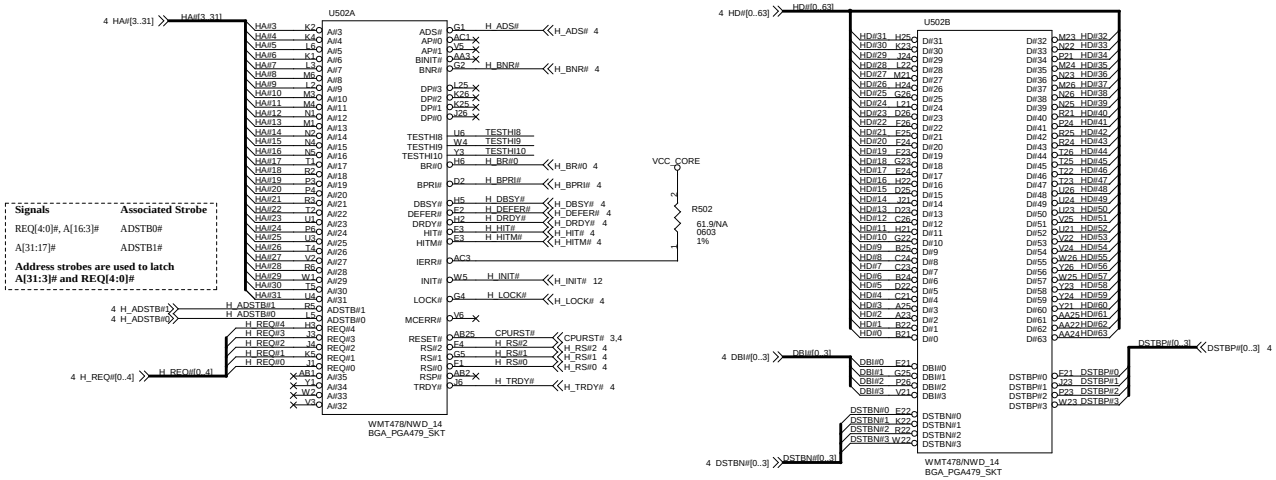
CPU(1)_NORTHWOOD



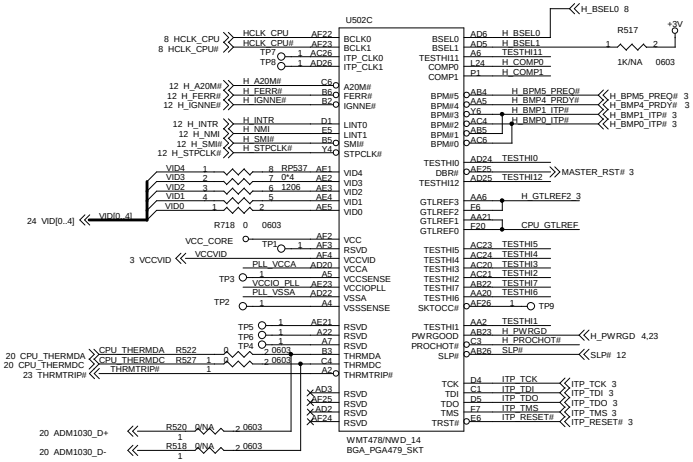
System Bus Frequency Select Signals

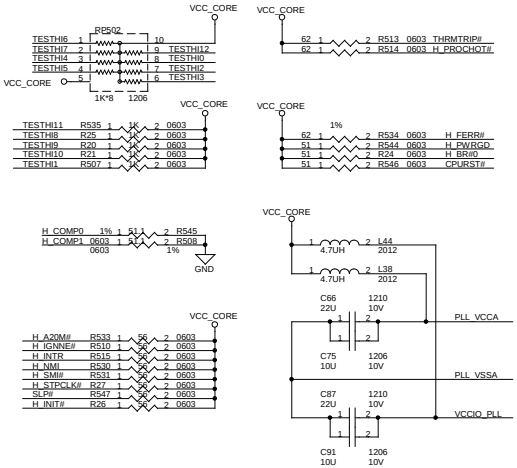
BSEL1	BSEL0	Function
L	L	100MHz
L	H	RESERVED
H	L	RESERVED
H	H	RESERVED

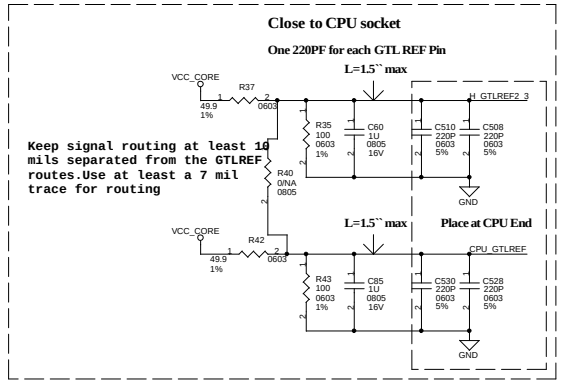
VID4	VID3	VID2	VID1	VID0	VOLT.
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	VRM output off

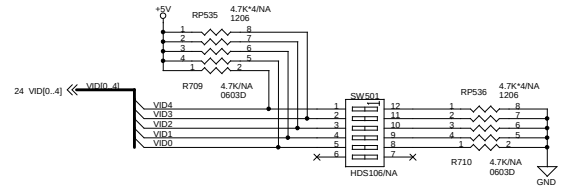
← Northwood CPU Voltage

check pull-up value









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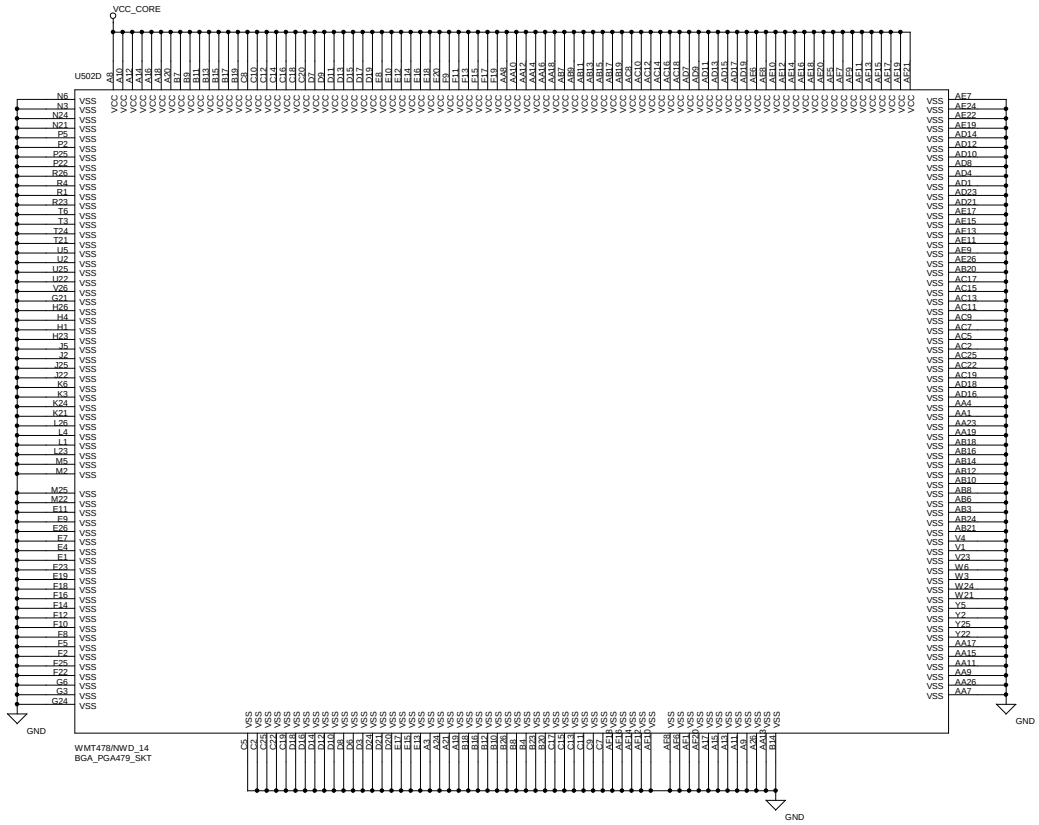
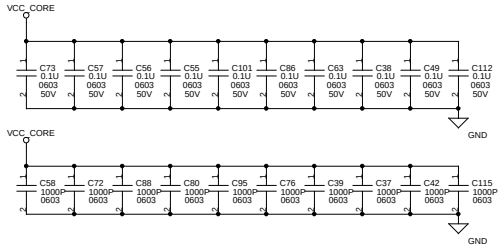
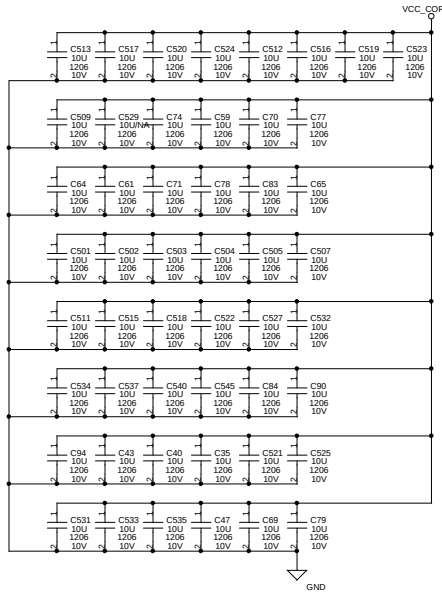
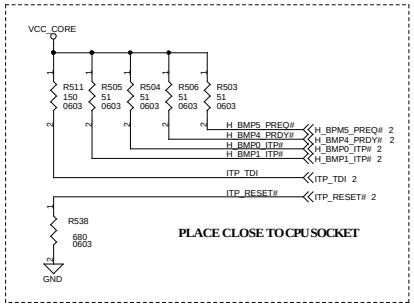
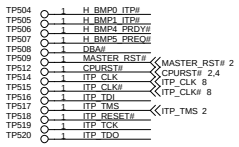
CPU(2)_NORTHWOOD

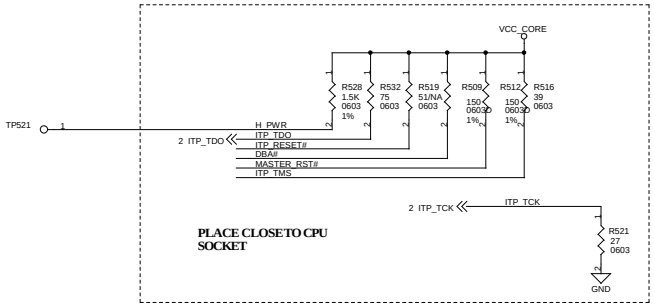


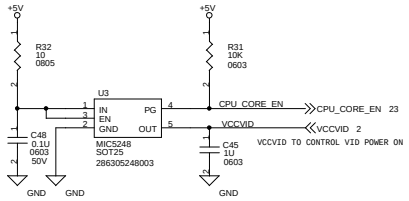












MiTAC

Title	8500	
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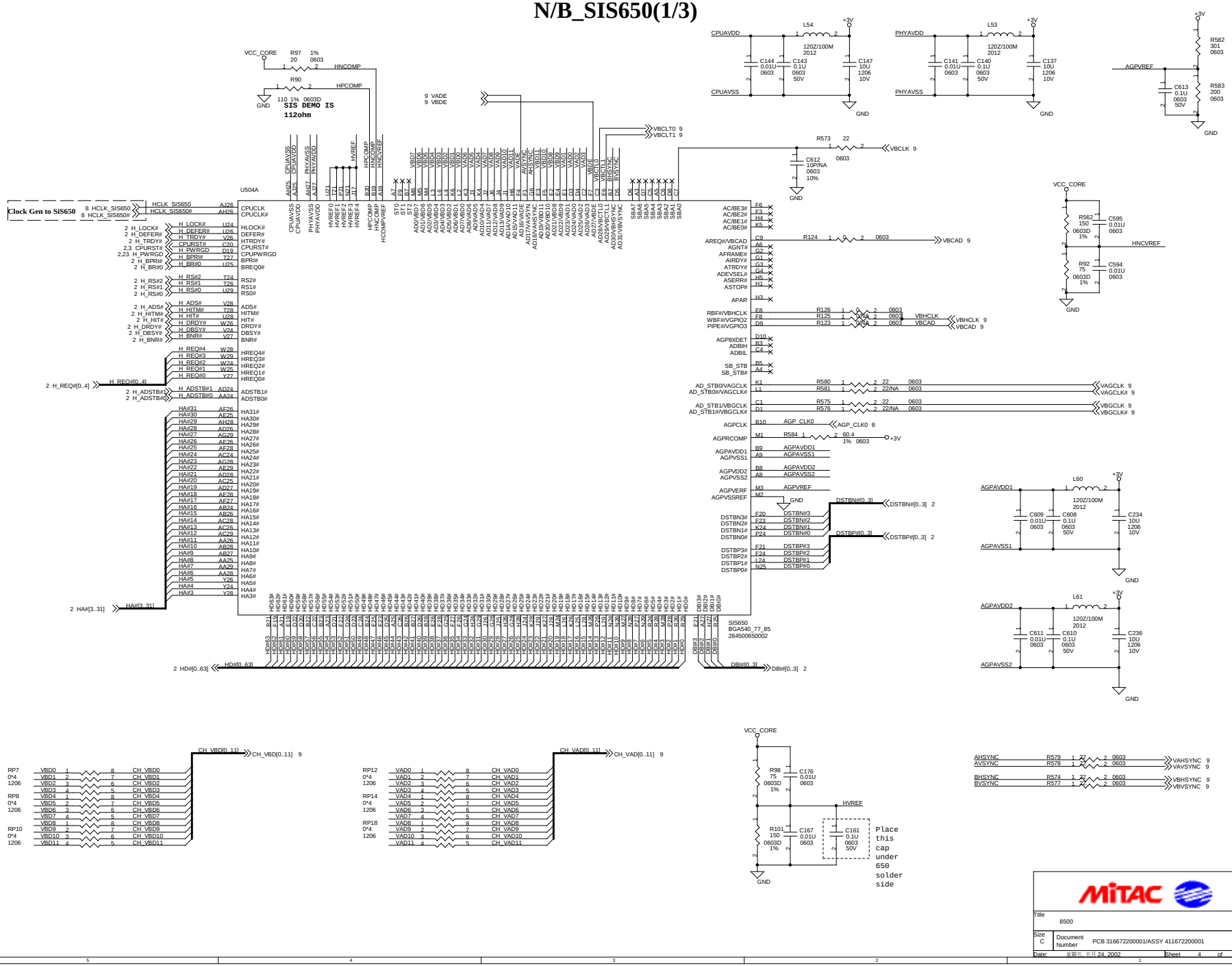
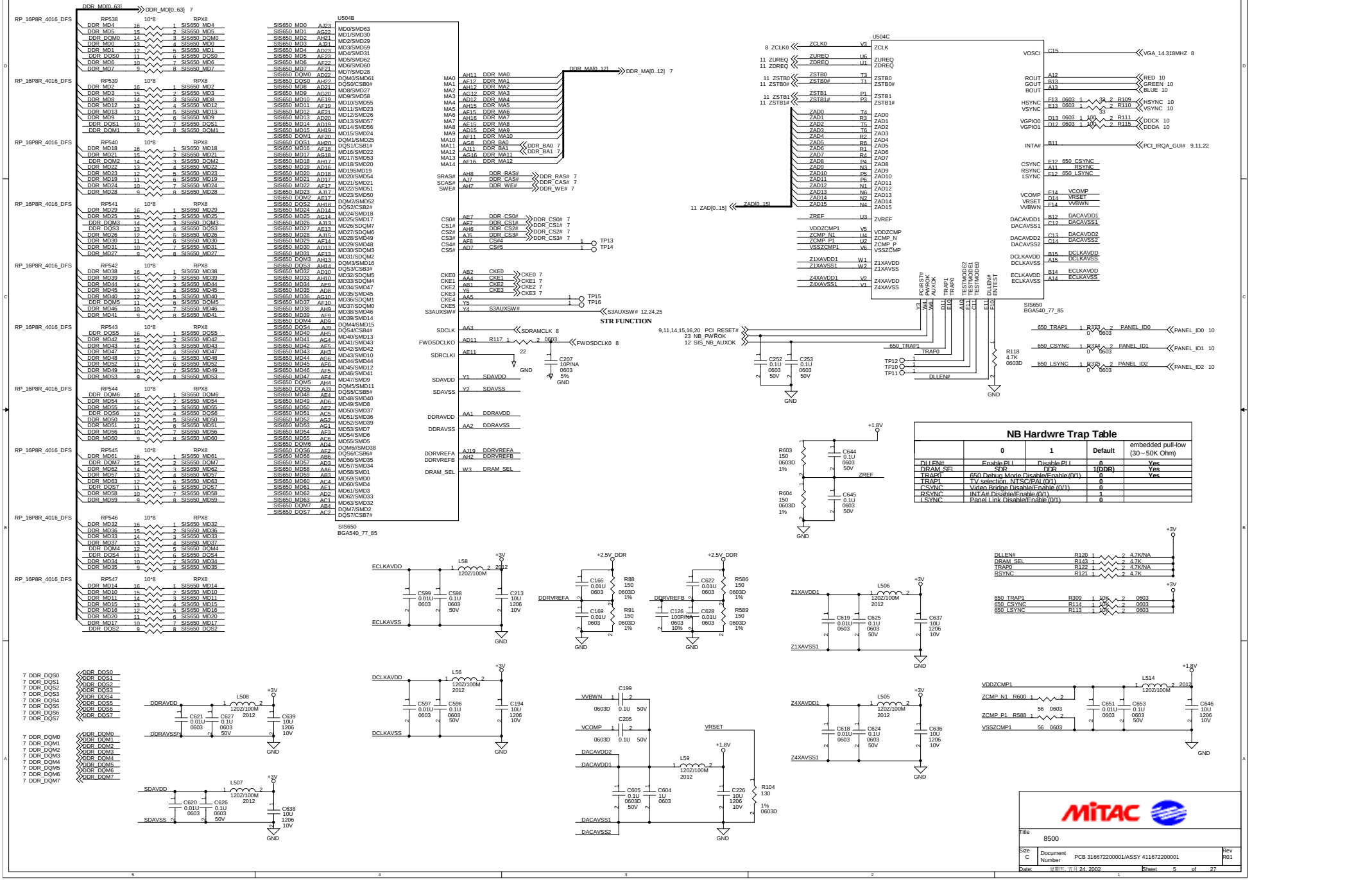
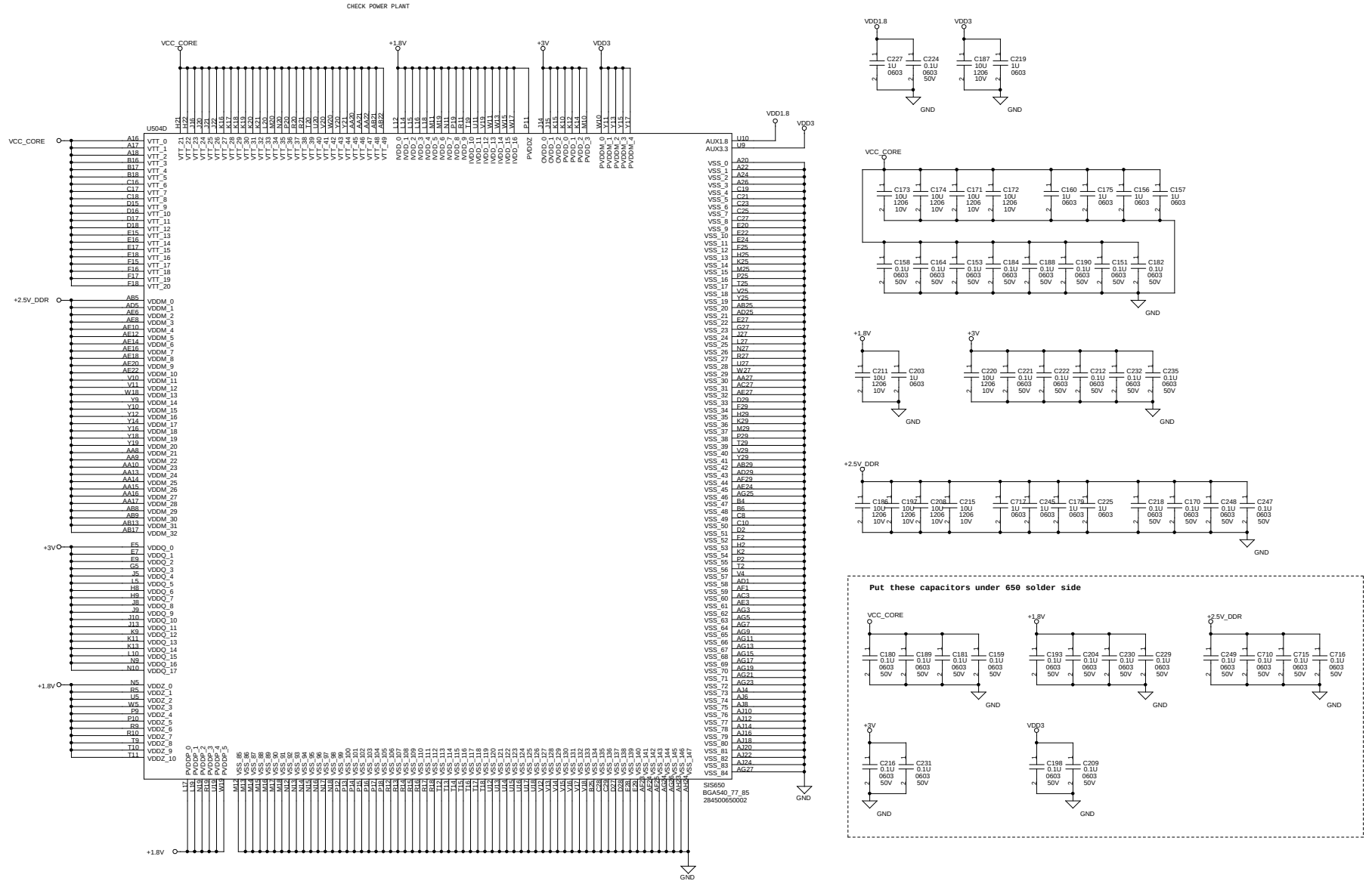
N/B_SIS650(1/3)



N/B_SIS650(2/3)



N/B_SIS650(3/3)



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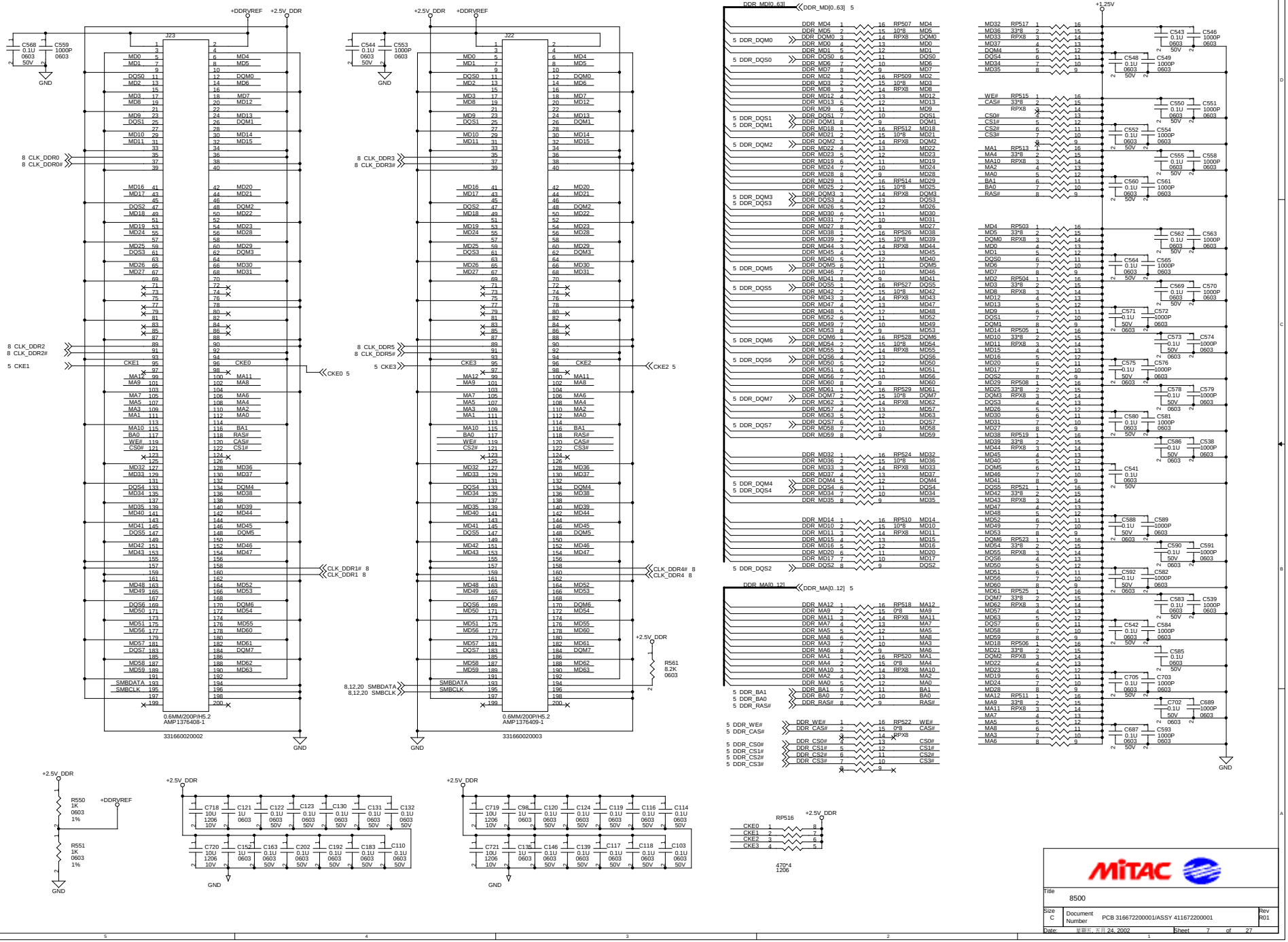
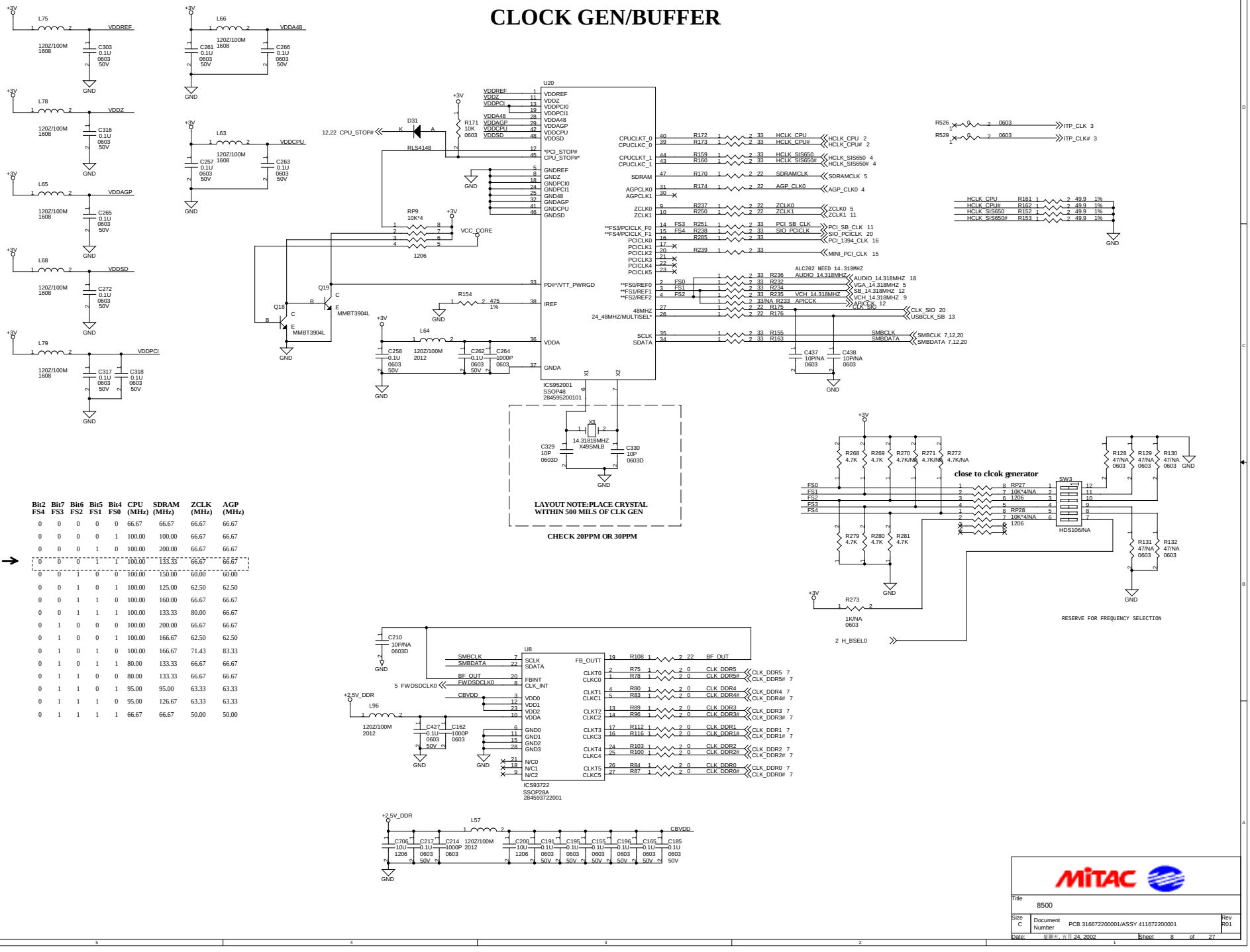
DDR SLOT AND TERMINATION



CLOCK GEN/BUFFER



Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGP (MHz)
0	0	0	0	0	66.67	66.67	66.67	66.67
0	0	0	0	1	100.00	100.00	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	100.00	150.00	60.00	60.00
0	0	1	0	1	100.00	125.00	62.50	62.50
0	0	1	1	0	100.00	160.00	66.67	66.67
0	0	1	1	1	100.00	133.33	80.00	66.67
0	1	0	0	0	100.00	200.00	66.67	66.67
0	1	0	0	1	100.00	166.67	62.50	62.50
0	1	0	1	0	100.00	166.67	71.43	83.33
0	1	0	1	1	80.00	133.33	66.67	66.67
0	1	1	0	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	1	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

MiTAC

Title	8500	
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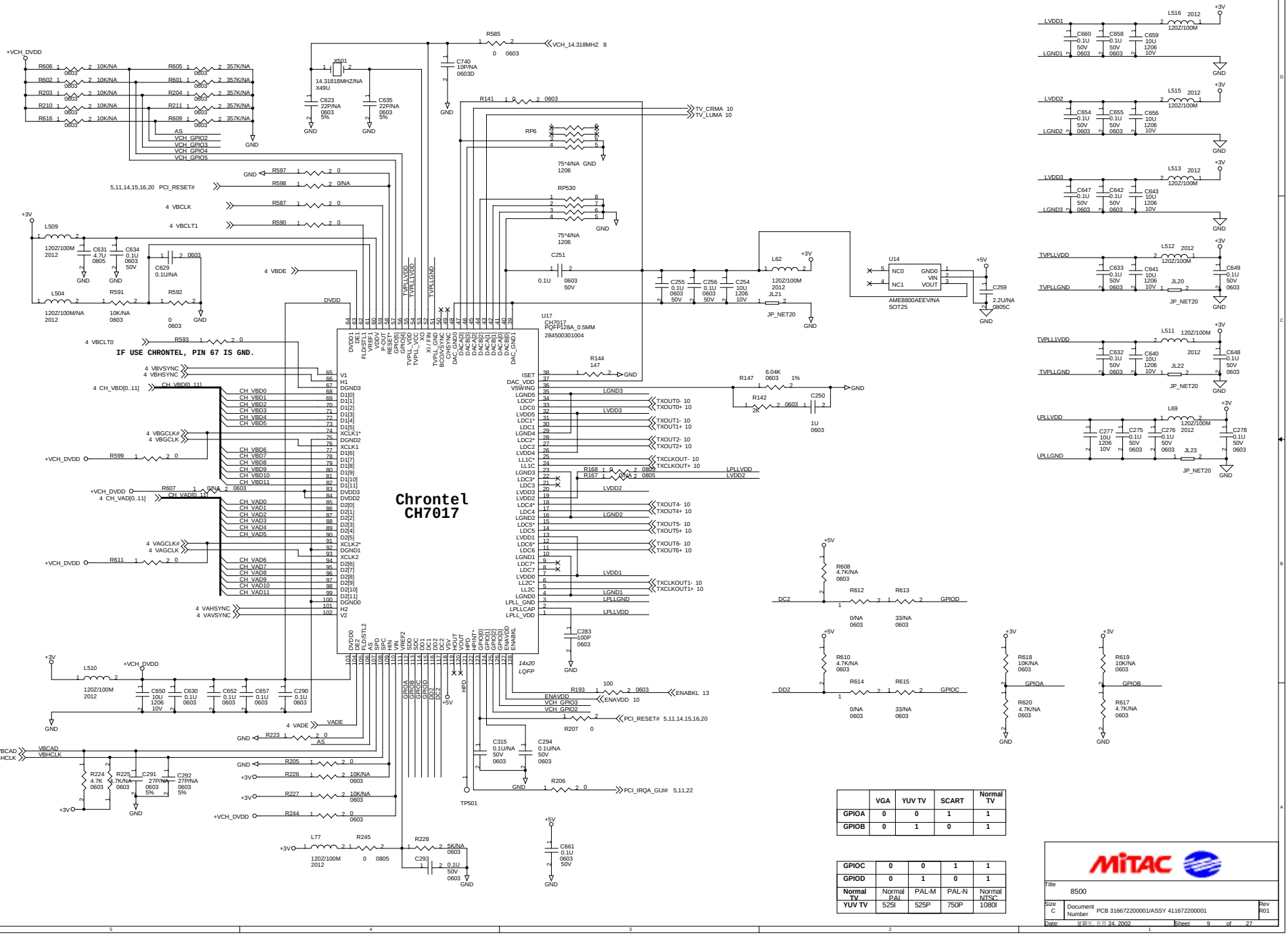
CH7017



	VGA	YUV TV	SCART	Normal TV
GPIOA	0	0	1	1
GPIOB	0	1	0	1

GPIOC	0	0	1	1
GPIOD	0	1	0	1
Normal TV	Normal PAL	PAL-M	PAL-N	Normal NTSC
YUV TV	525I	525P	750P	1080I

MiTAC

Title: 8500

Size: C | Document Number: PCB 316672200001/ASSY 411672200001 | Rev: R01

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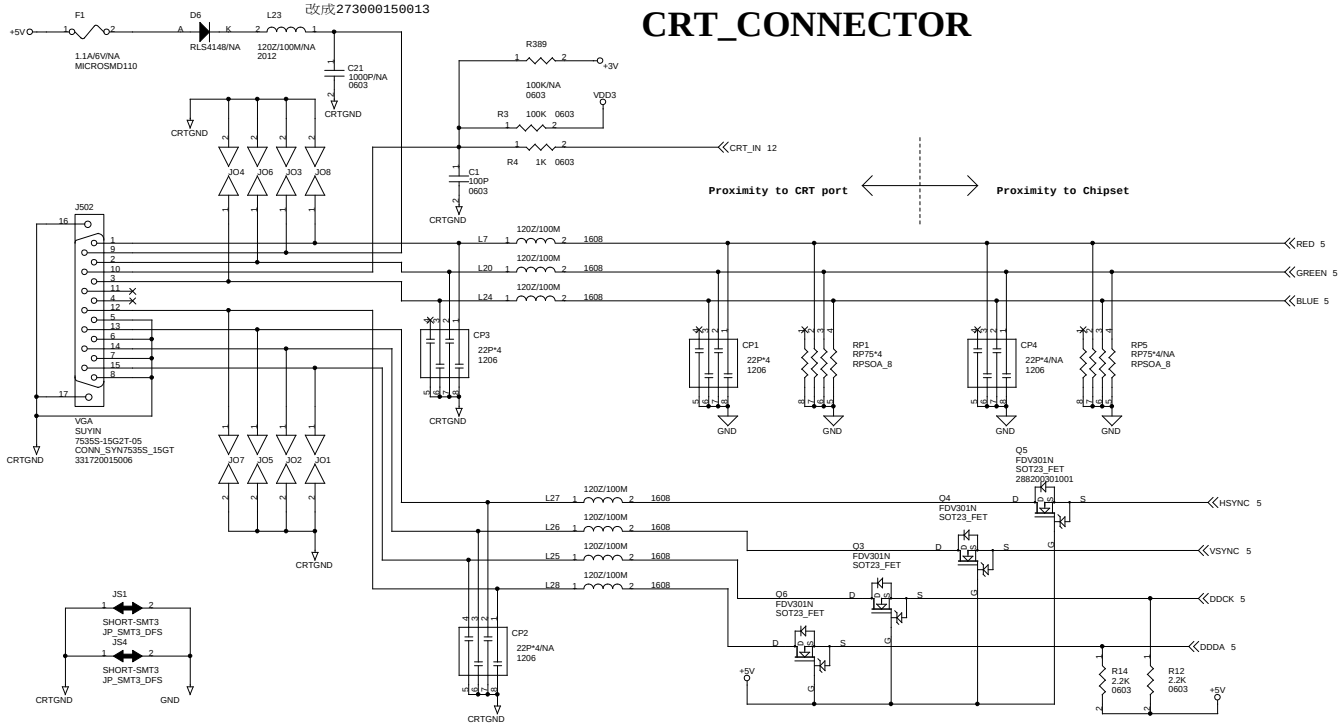
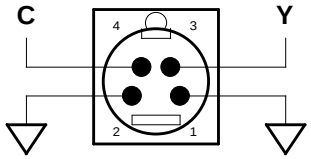
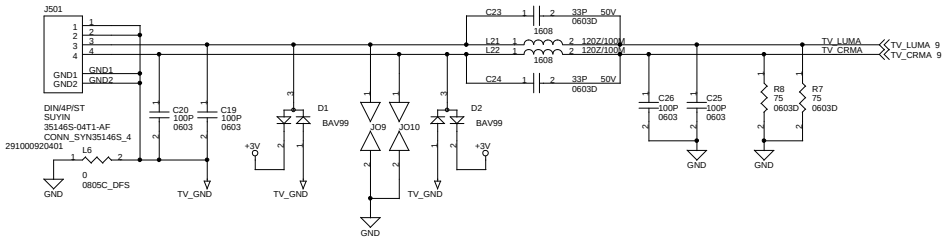
CRT_CONNECTOR



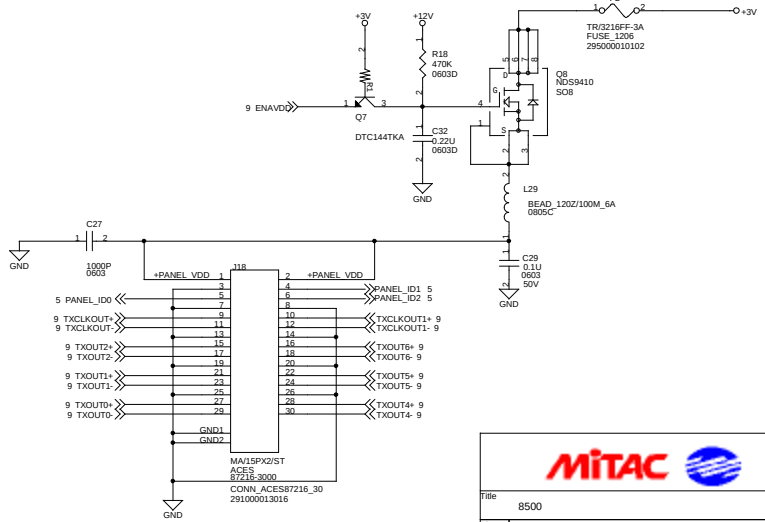
Pin#	Standard VGA
1	Red video
2	Green video
3	Blue video
4	Monitor ID bit 2
5	Test (ground)
6	Red video return
7	Green video return
8	Blue video return
9	No connection (mechanical key)
10	Sync. return
11	Monitor ID bit 0
12	Monitor ID bit 1
13	Horizontal sync.
14	Vertical sync.
15	Monitor ID bit 3

TV/S-JACK





LCD CONNECTOR



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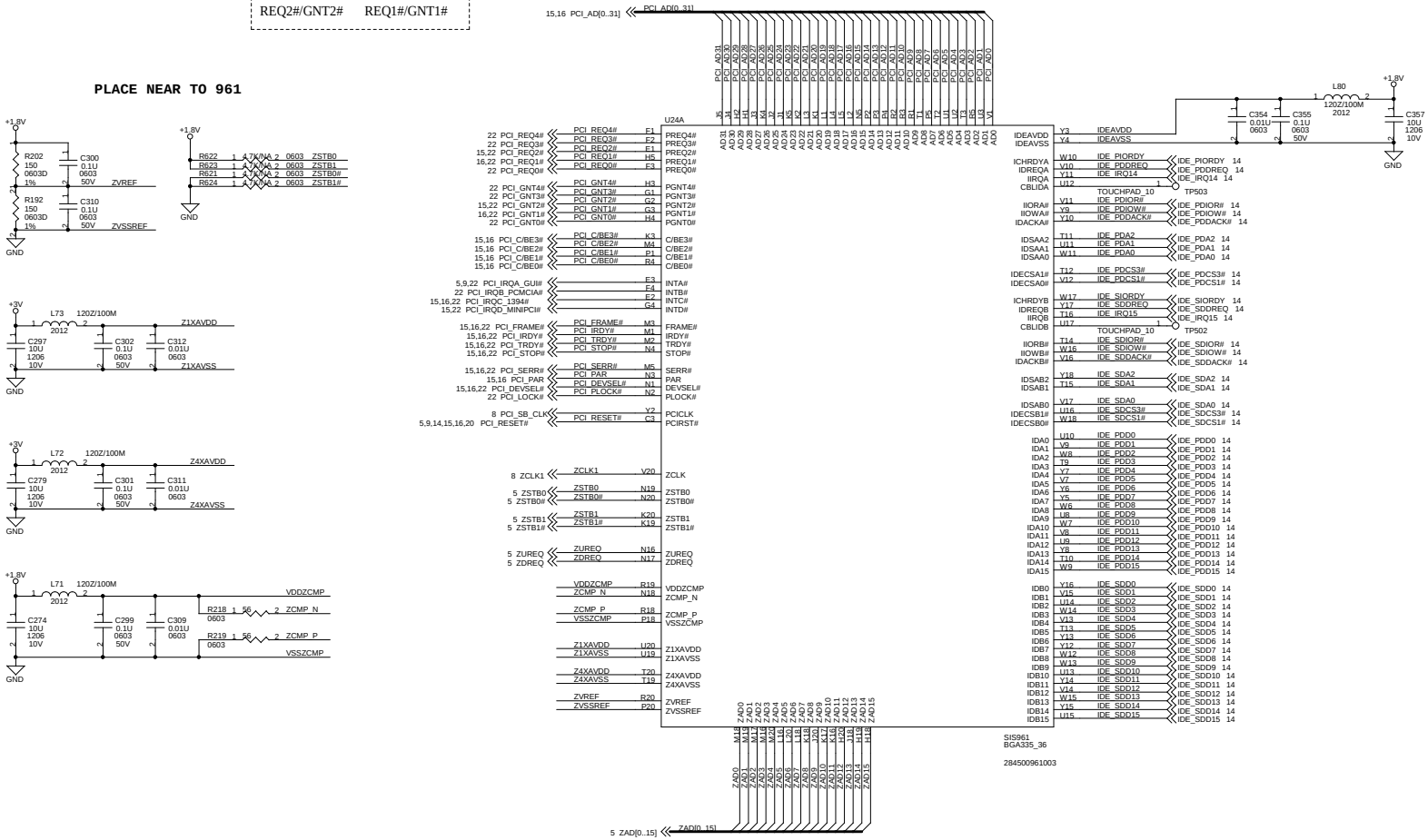
CHANGE TO TI 74LV164A P/N:282074164002

SiS961(1/3)

MINI-PCI	IEEE1394
AD21	AD22
PCI_INTD#	PCI_INTC#
REQ2#/GNT2#	REQ1#/GNT1#

PLACE NEAR TO 961



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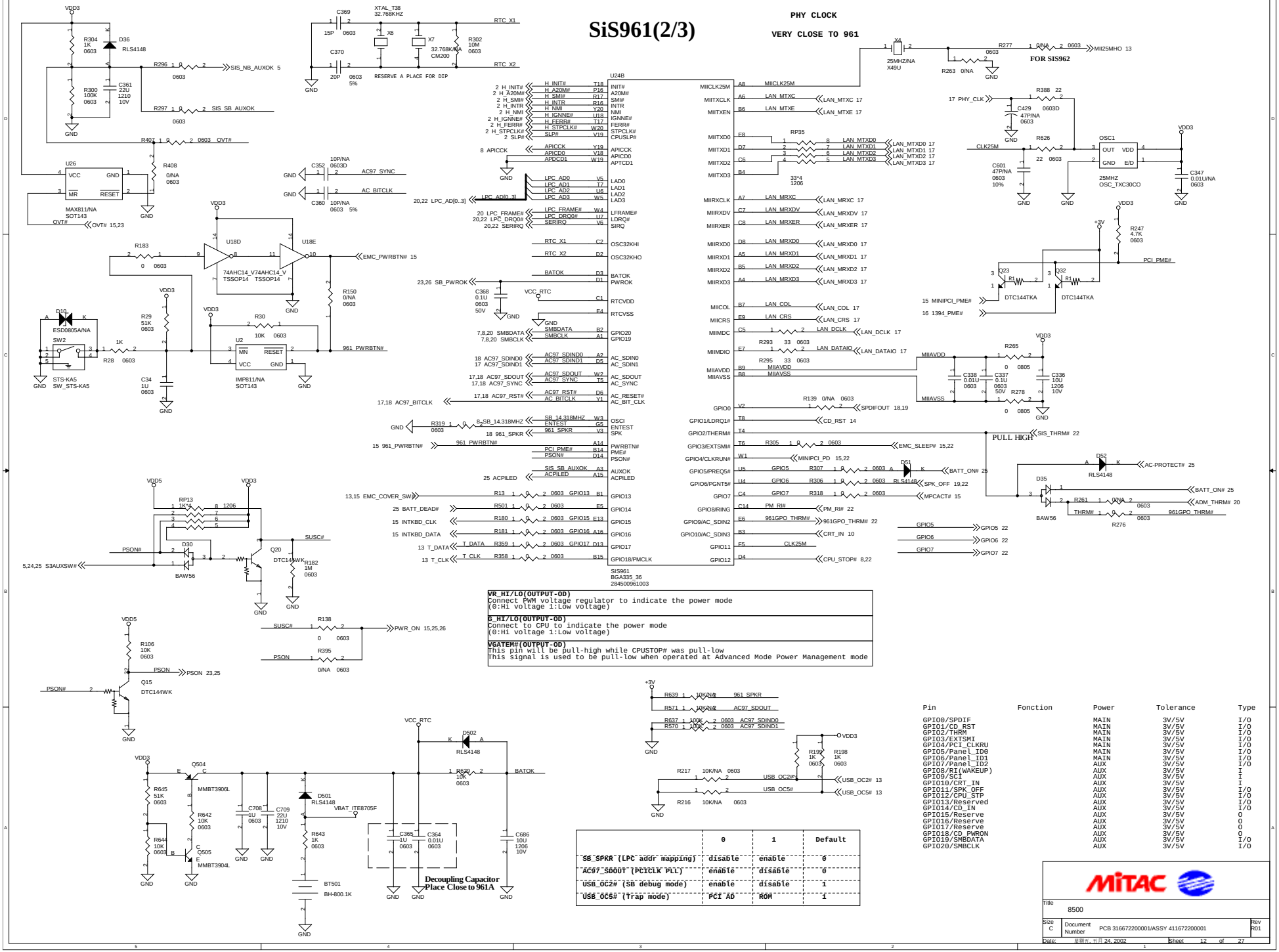
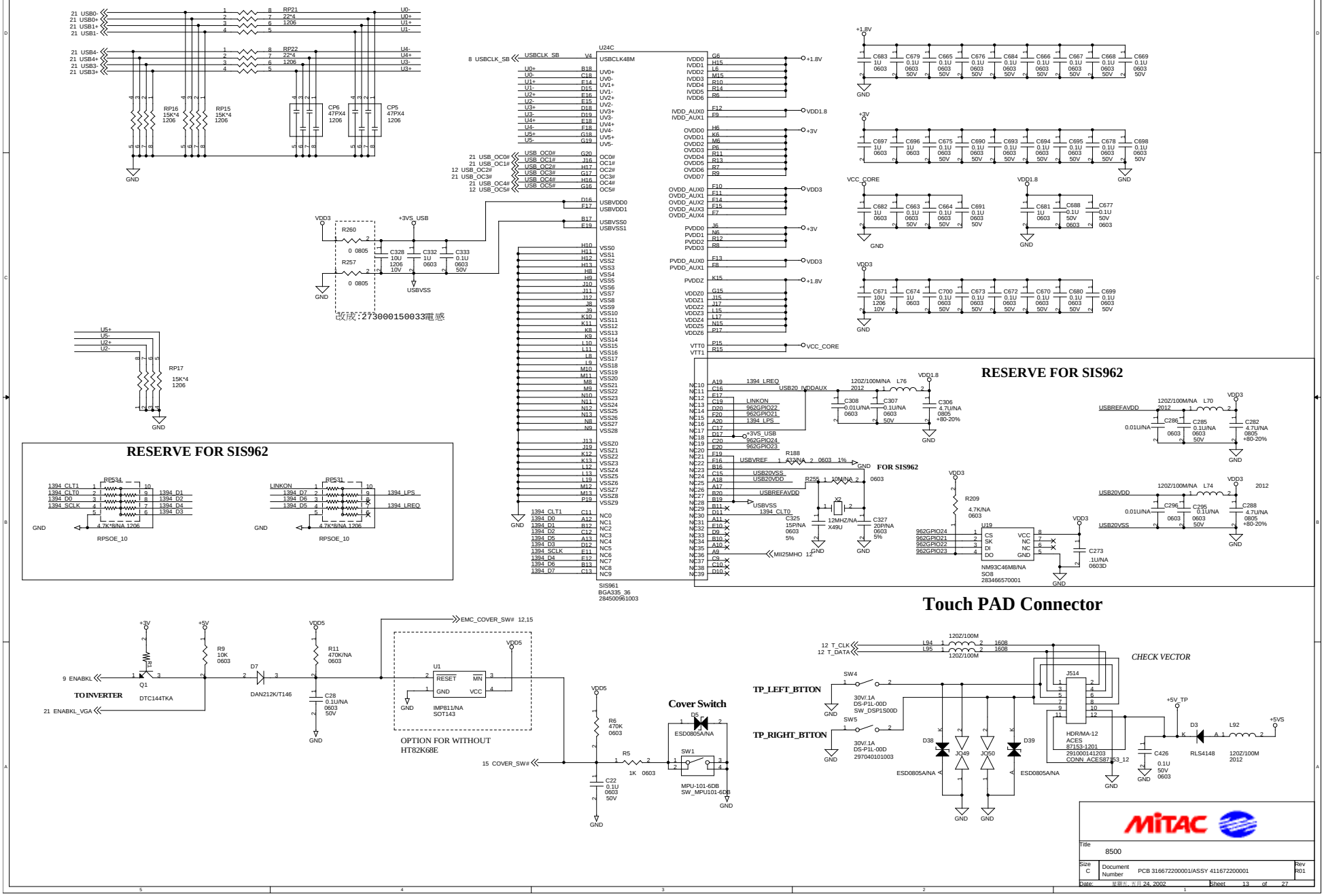


Pin	Fonction	Power	Tolerance	Type
GPIO0/SPDIF		MAIN	3V/5V	I/O
GPIO1/CD_RST		MAIN	3V/5V	I/O
GPIO2/THRM		MAIN	3V/5V	I/O
GPIO3/EXTSMI		MAIN	3V/5V	I/O
GPIO4/PCI_CLKRU		MAIN	3V/5V	I/O
GPIO5/Panel_ID0		MAIN	3V/5V	I/O
GPIO6/Panel_ID1		MAIN	3V/5V	I/O
GPIO7/Panel_ID2		AUX	3V/5V	I/O
GPIO8/RI(WAKEUP)		AUX	3V/5V	I
GPIO9/SCI		AUX	3V/5V	I
GPIO10/CRT_IN		AUX	3V/5V	I
GPIO11/SPK_OFF		AUX	3V/5V	I/O
GPIO12/CPU_STP		AUX	3V/5V	I/O
GPIO13/Reserved		AUX	3V/5V	I/O
GPIO14/CD_IN		AUX	3V/5V	I/O
GPIO15/Reserve		AUX	3V/5V	O
GPIO16/Reserve		AUX	3V/5V	O
GPIO17/Reserve		AUX	3V/5V	O
GPIO18/CD_PWRON		AUX	3V/5V	O
GPIO19/SMBDATA		AUX	3V/5V	I/O
GPIO20/SMBCLK		AUX	3V/5V	I/O

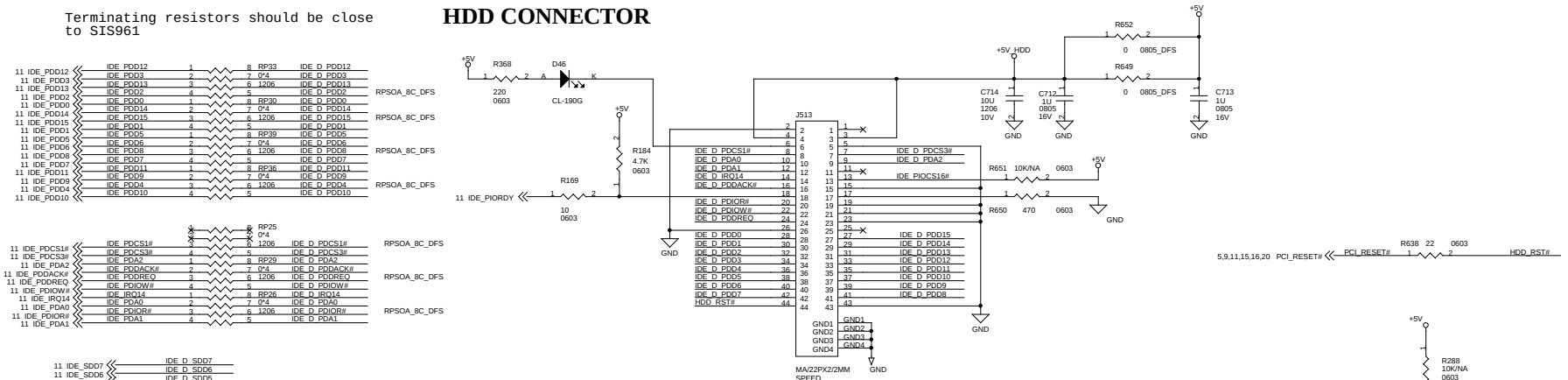
	0	1	Default
SB_SPKR (LPC addr mapping)	disable	enable	0
AC97_SDOUT (PCICLK PLL)	enable	disable	0
USB_OC2# (SB debug mode)	enable	disable	1
USB_OC5# (Trap mode)	PCI AD	ROM	1

SiS961(3/3)

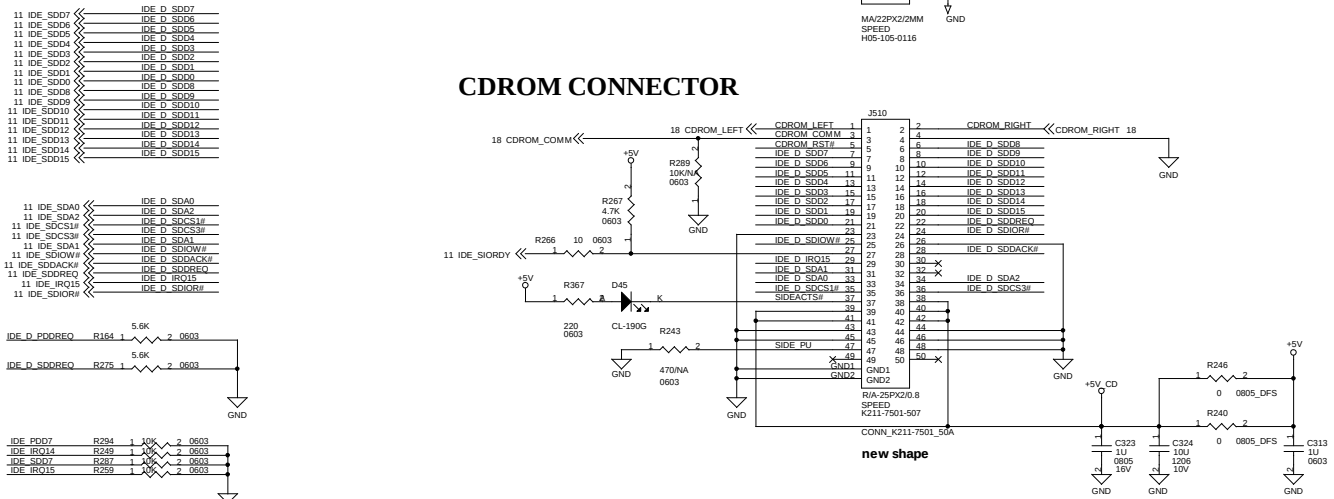


Terminating resistors should be close to SIS961

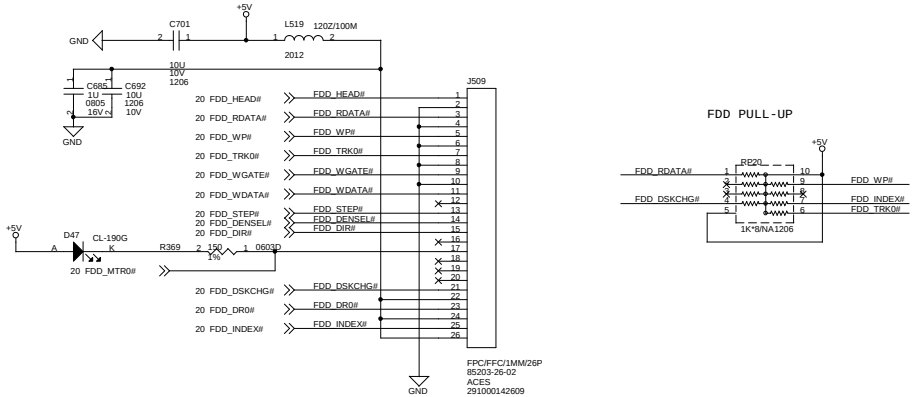
HDD CONNECTOR



CDROM CONNECTOR



FLOPPY CONNECTOR



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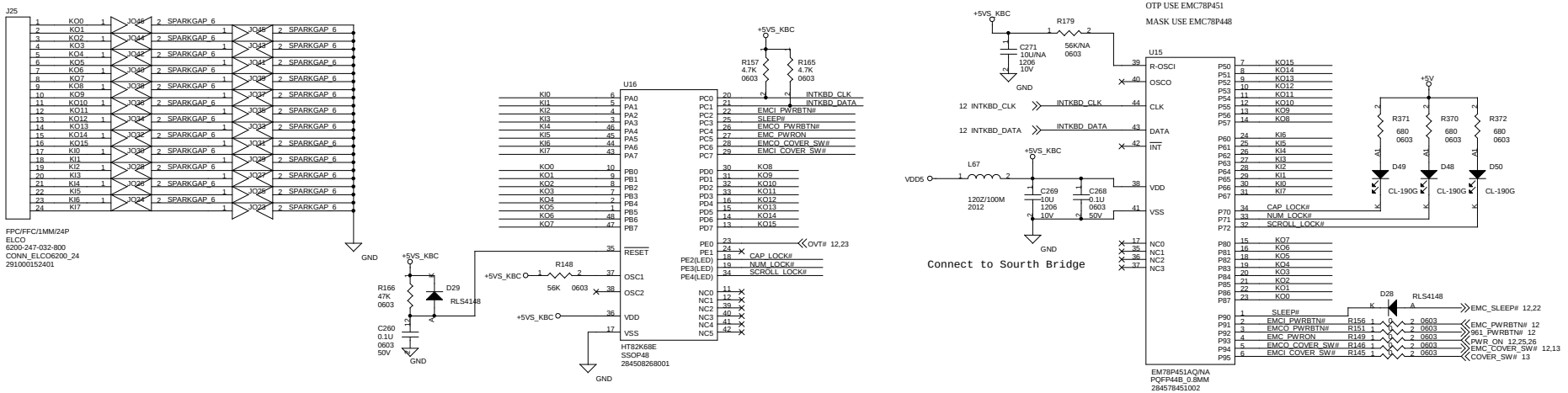
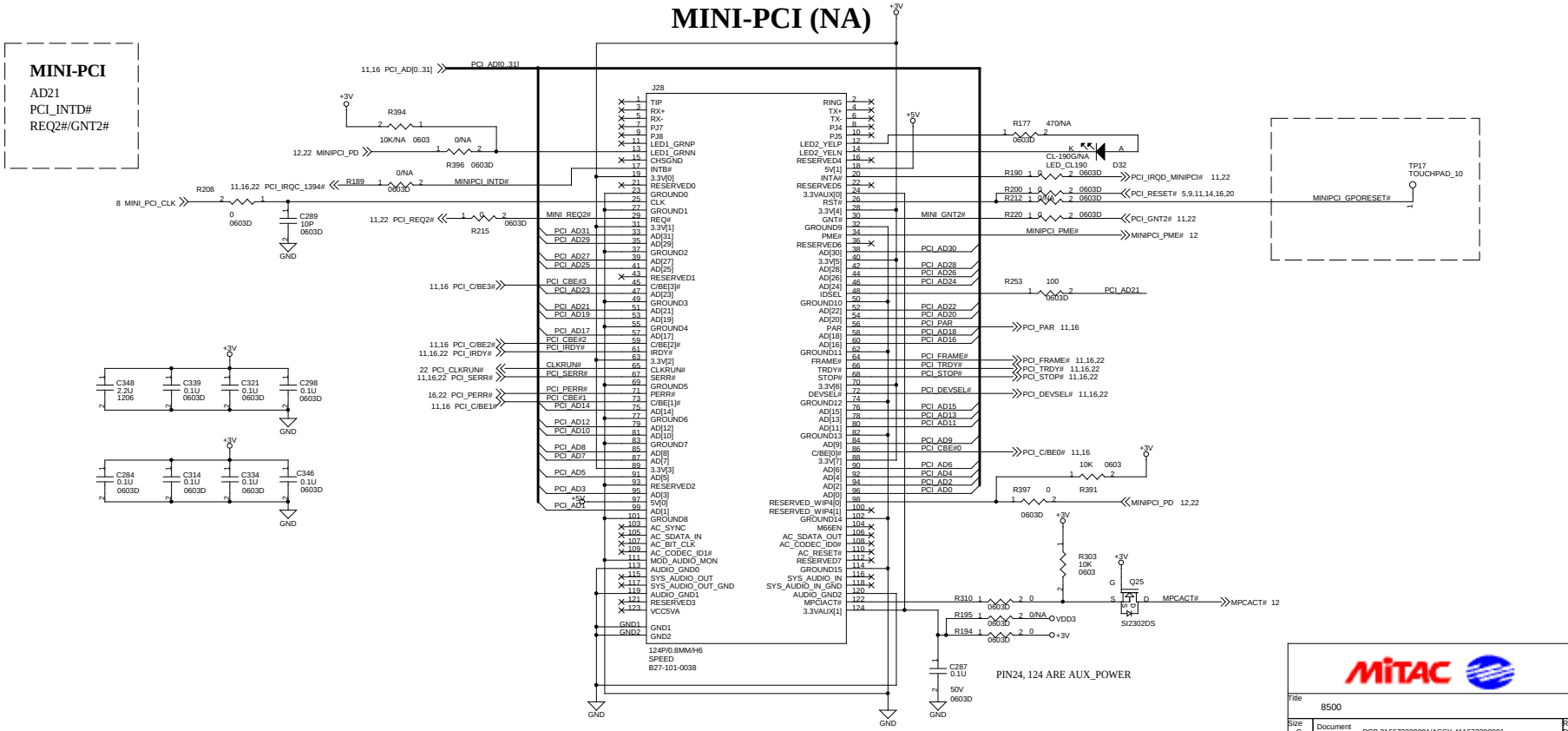
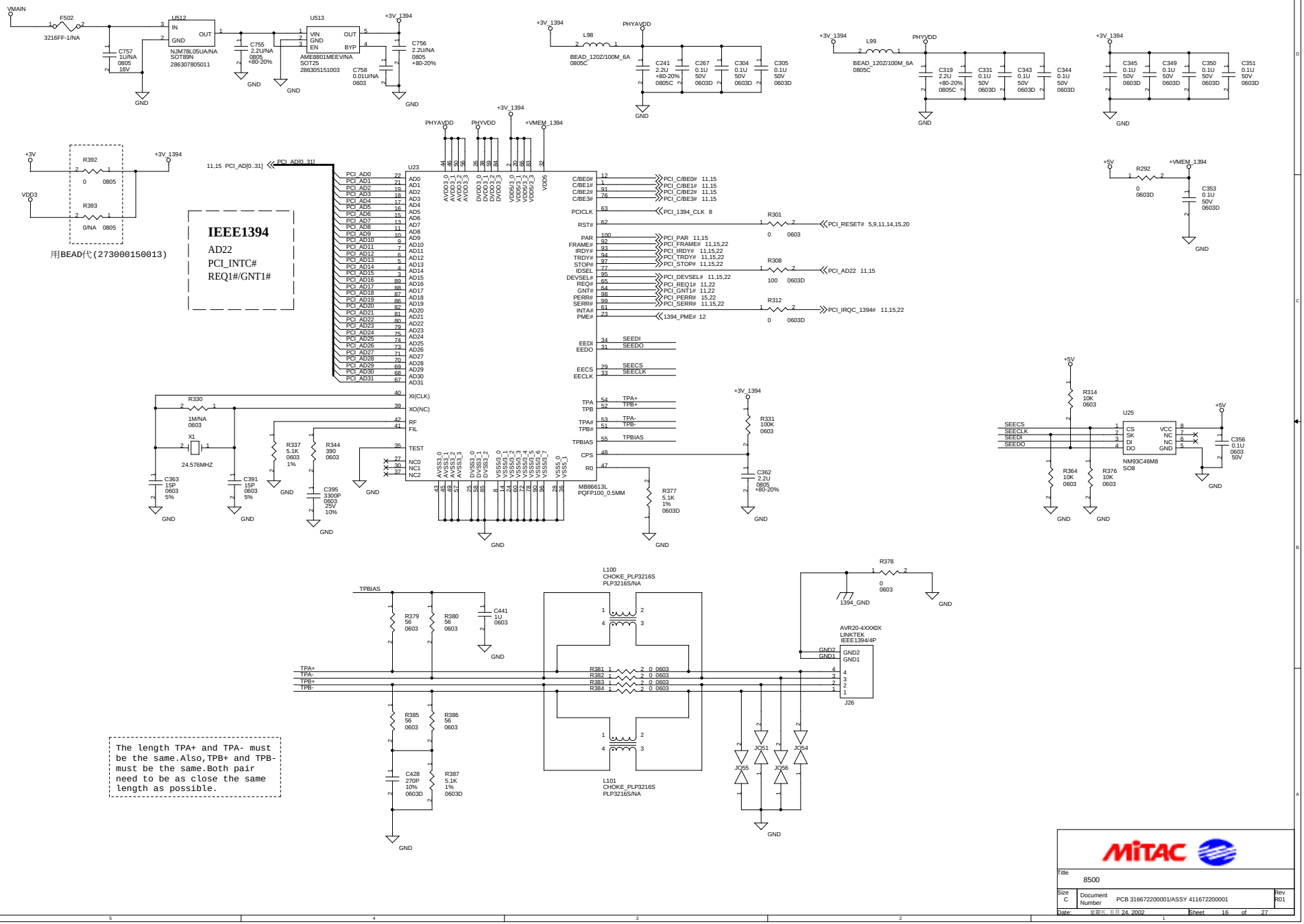
INTERNAL KEYBOARD ENCODER



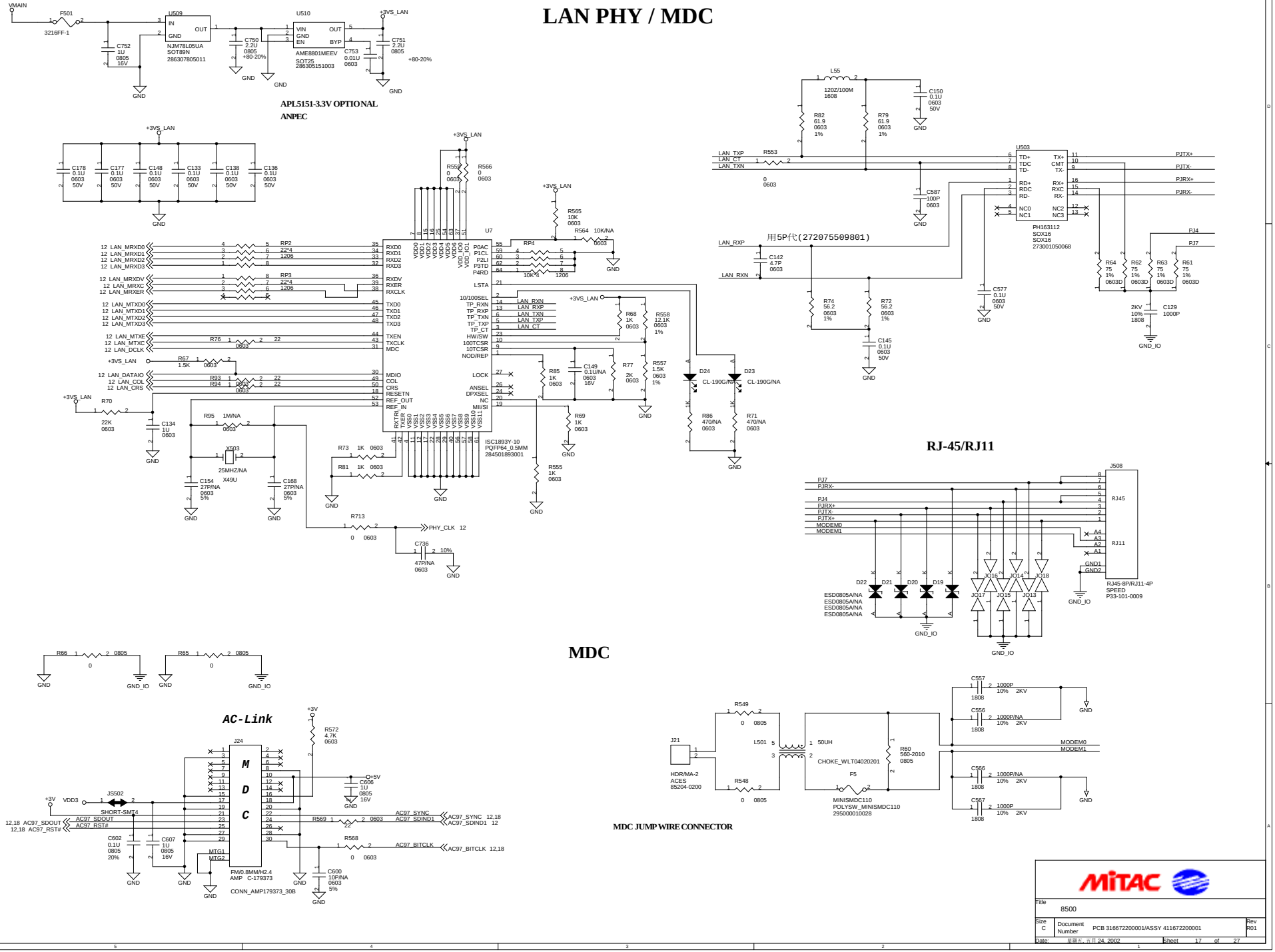
MINI-PCI (NA)



IEEE1394-MB86613S



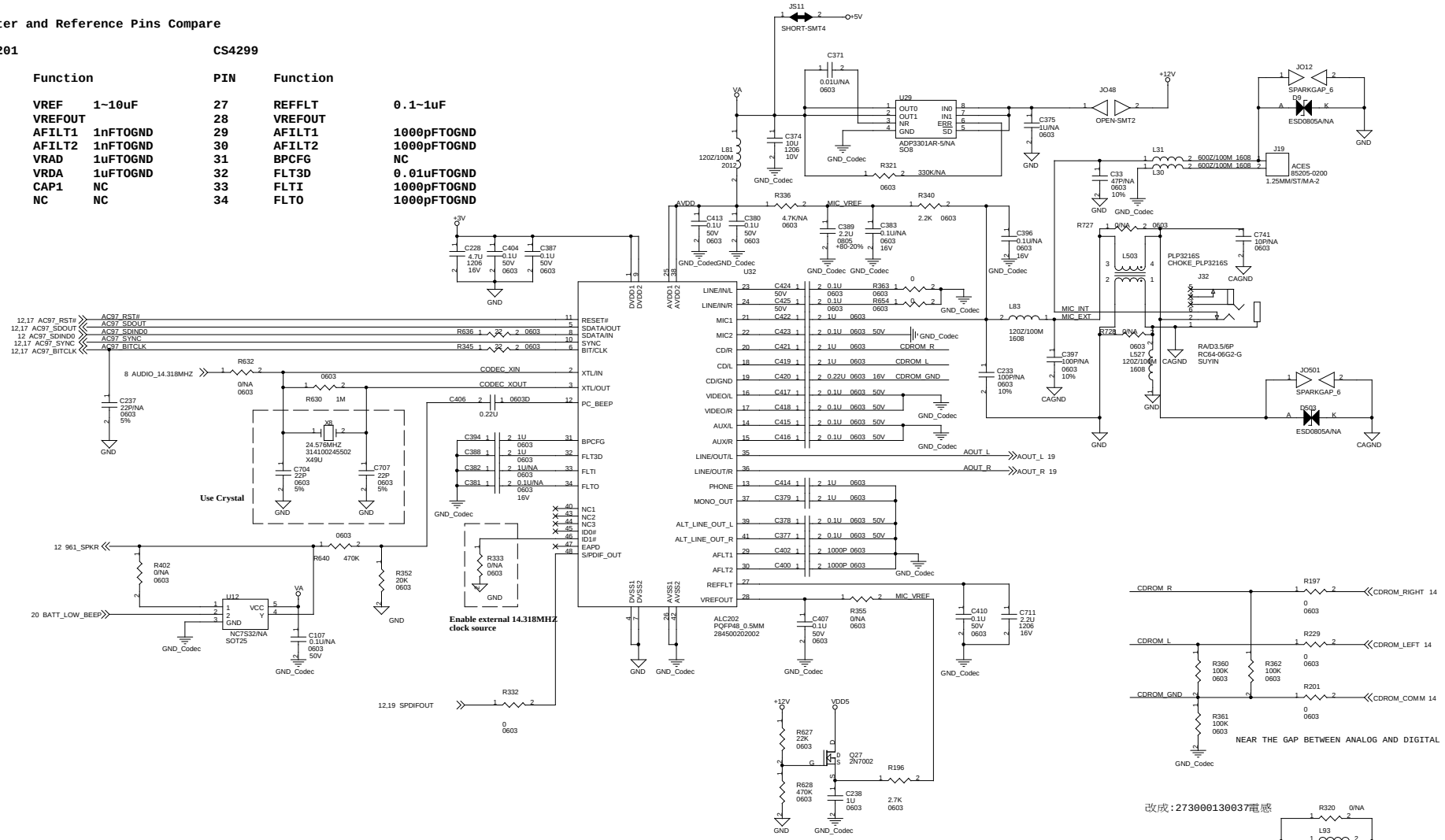
LAN PHY / MDC



AUDIO CODEC(ALC201)

Filter and Reference Pins Compare

ALC201			CS4299		
PIN	**Function**		**PIN**	**Function**	
27	**VREF**	**1~10uF**	**27**	**REFFLT**	**0.1~1uF**
28	**VREFOUT**		**28**	**VREFOUT**	
29	**AFILT1**	**1nFTOGND**	**29**	**AFILT1**	**1000pFTOGND**
30	**AFILT2**	**1nFTOGND**	**30**	**AFILT2**	**1000pFTOGND**
31	**VRAD**	**1uFTOGND**	**31**	**BPCFG**	**NC**
32	**VRDA**	**1uFTOGND**	**32**	**FLT3D**	**0.01uFTOGND**
33	**CAP1**	**NC**	**33**	**FLTI**	**1000pFTOGND**
34	**NC**	**NC**	**34**	**FLTO**	**1000pFTOGND**



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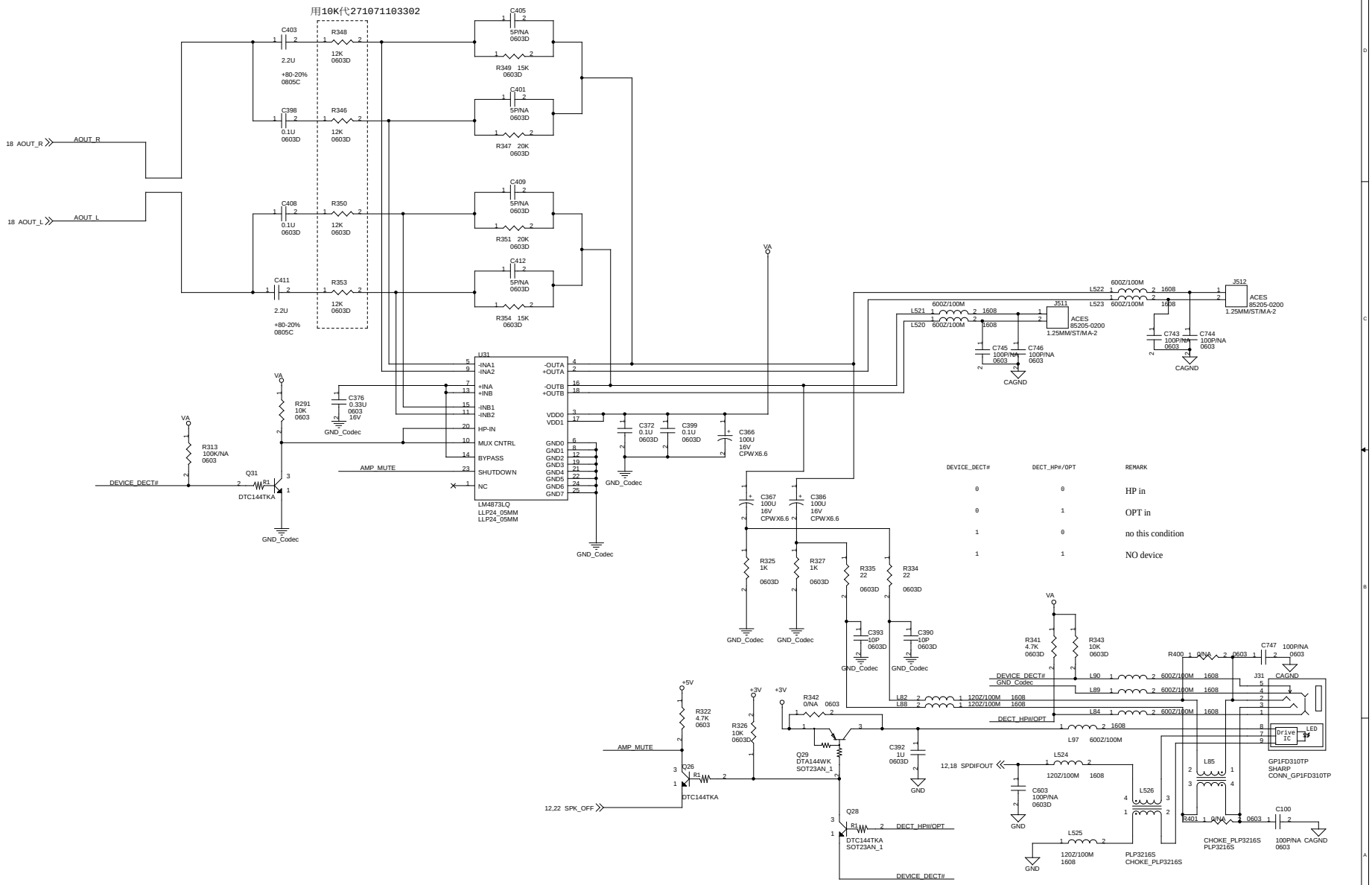
AUDIO AMPLIFIER - TPA0202



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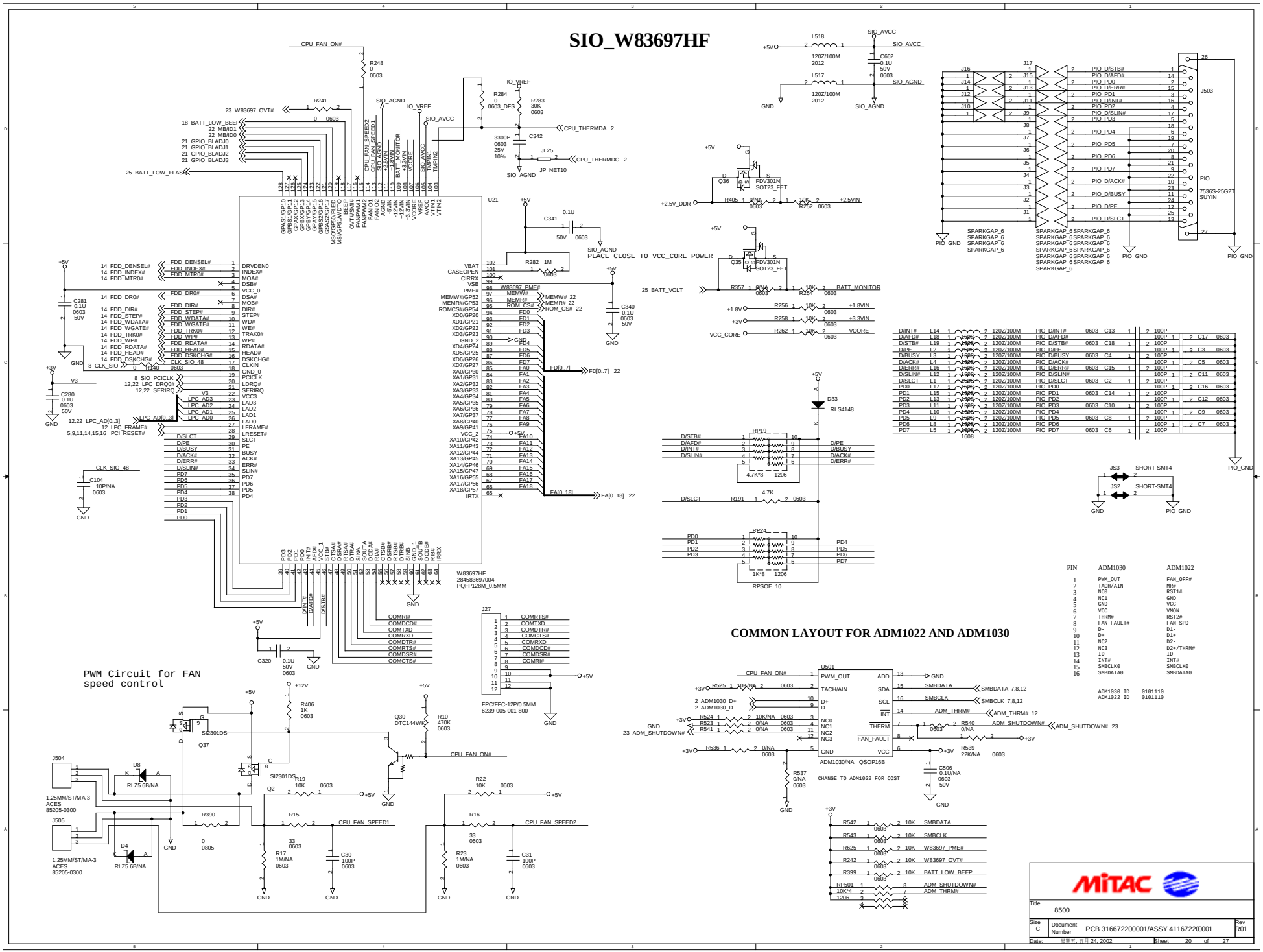
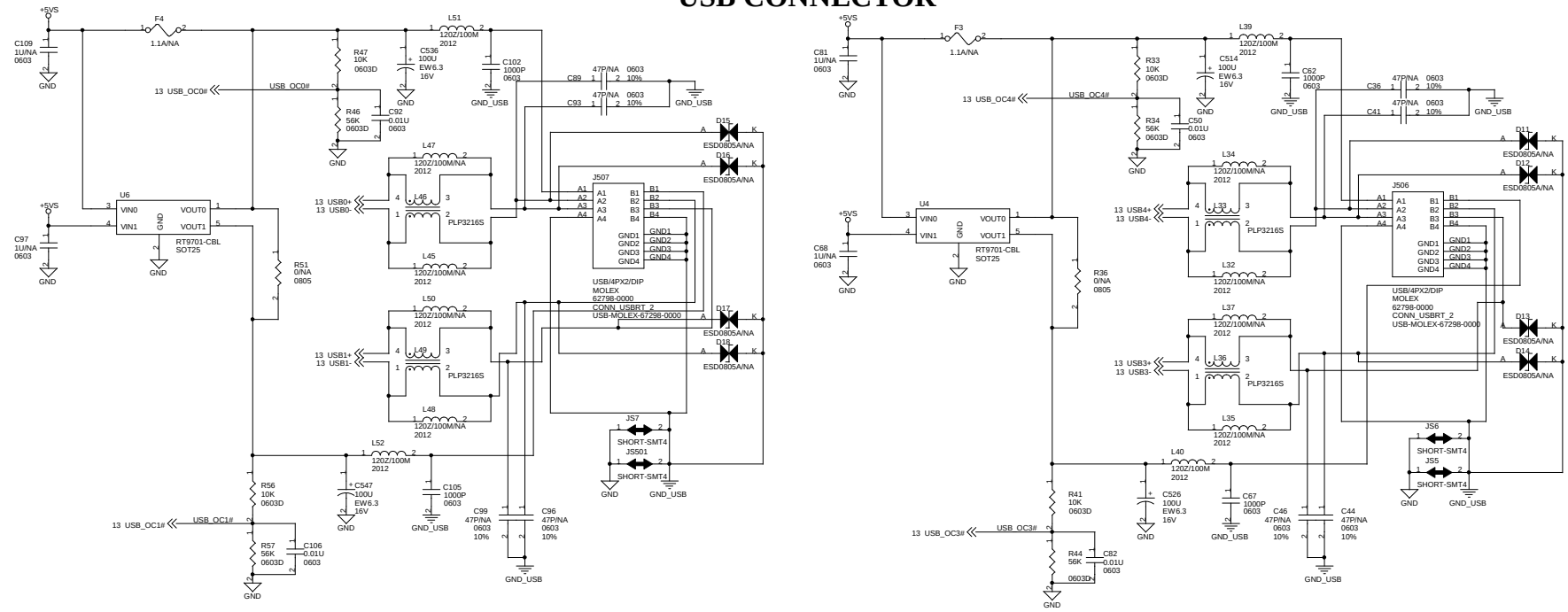
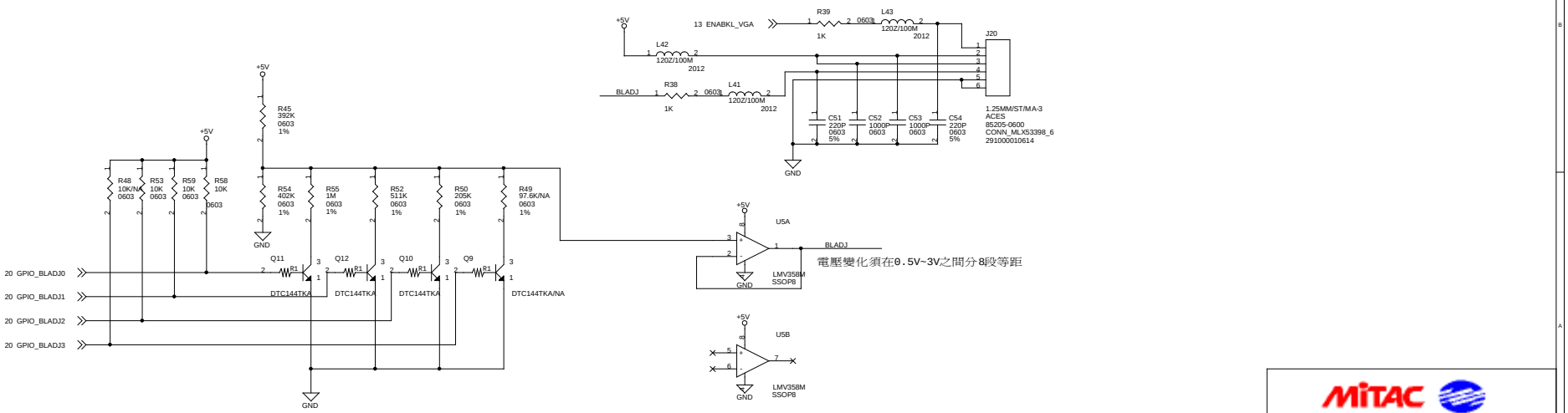


USB CONNECTOR



BACKLITE CONNECTOR



MiTAC

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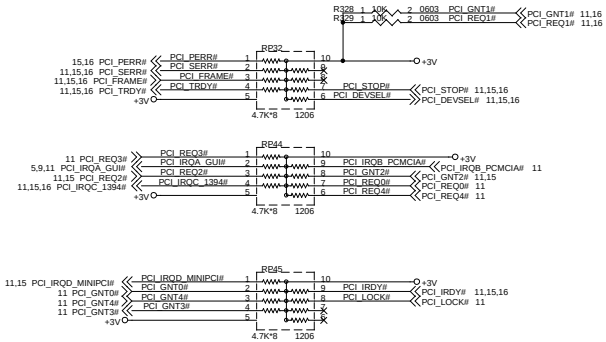
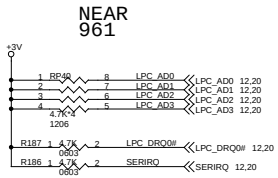
PULL UP

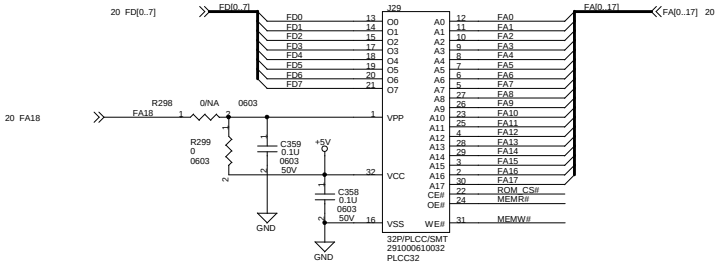
PCI PULL UP



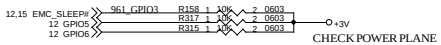
LPC UP



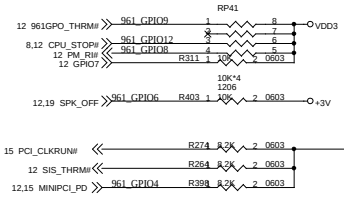
SYSTEM BIOS



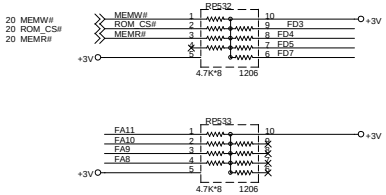
SiS961 GPIO PULL UP



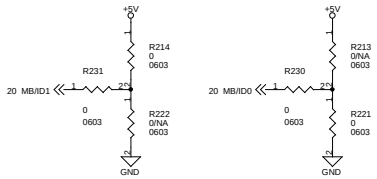
CHECK POWER PLANE



X-BUS PULL UP



W83697 GPIO PULL UP



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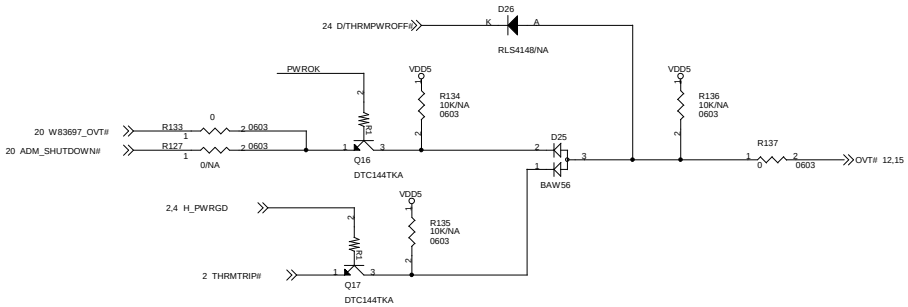
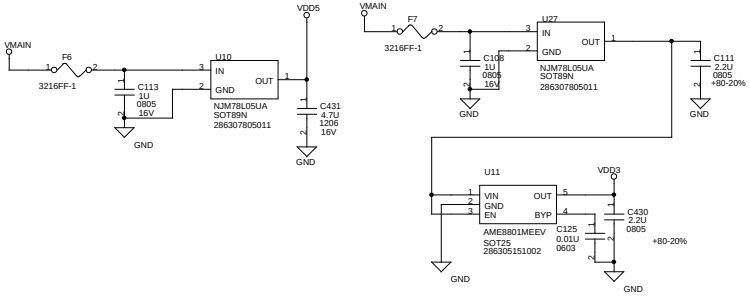
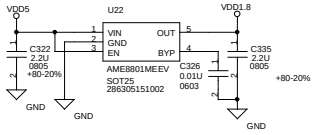
POWER PERIPHERIAL



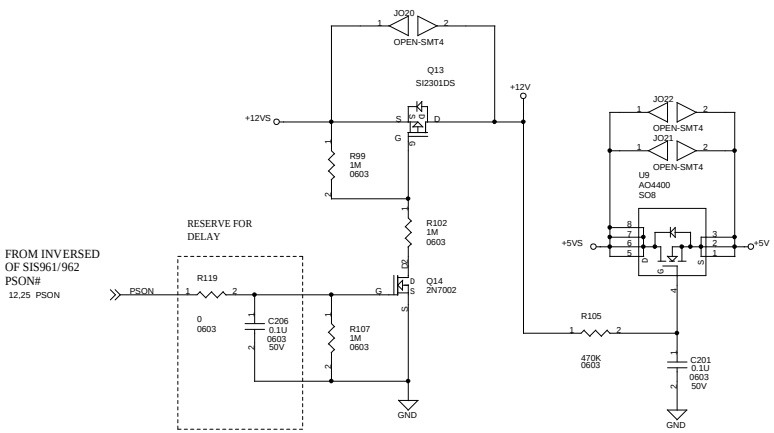
RESUME WELL POWER

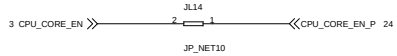


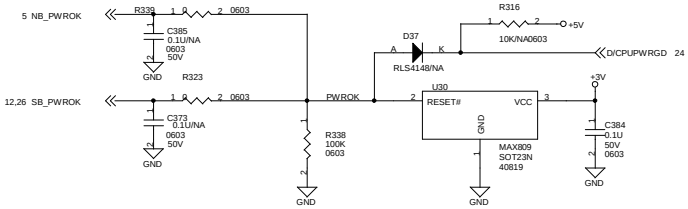
APL5151-3.3V OPTIONAL



APL5151-1.8V OPTIONAL
ANPEC







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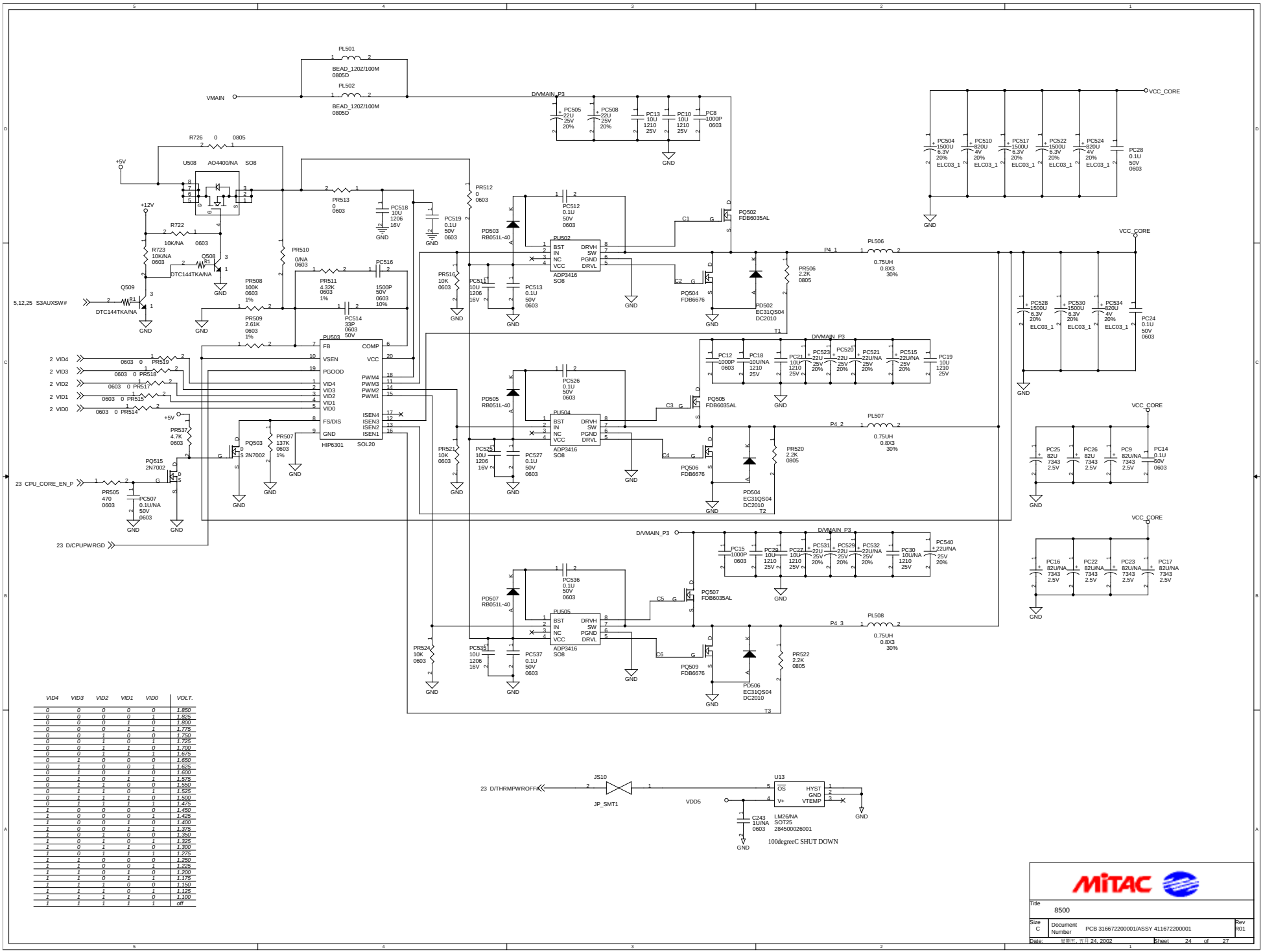

VID4	VID3	VID2	VID1	VID0	VOLT.
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	off

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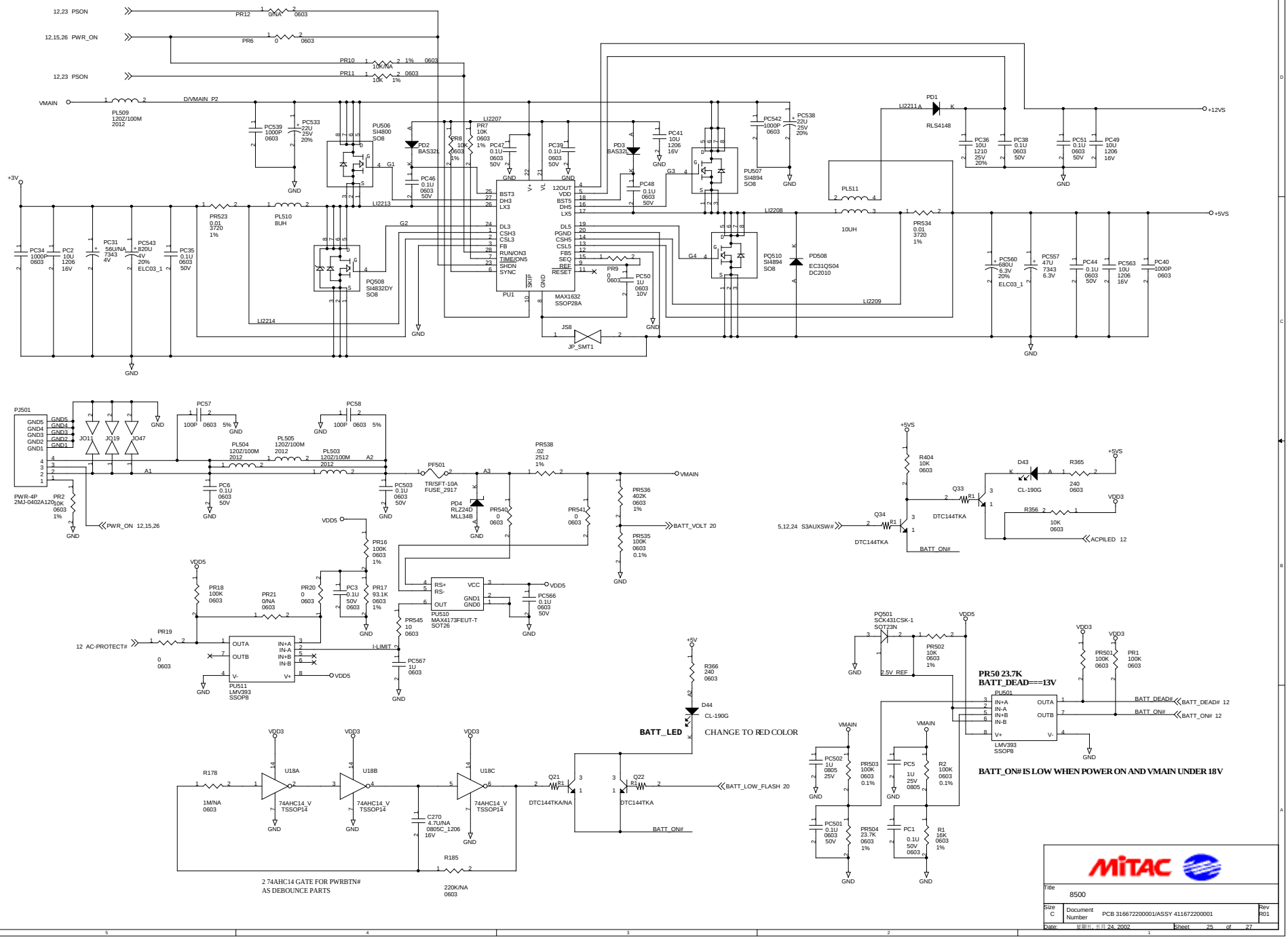
+3V/+5V/+12V



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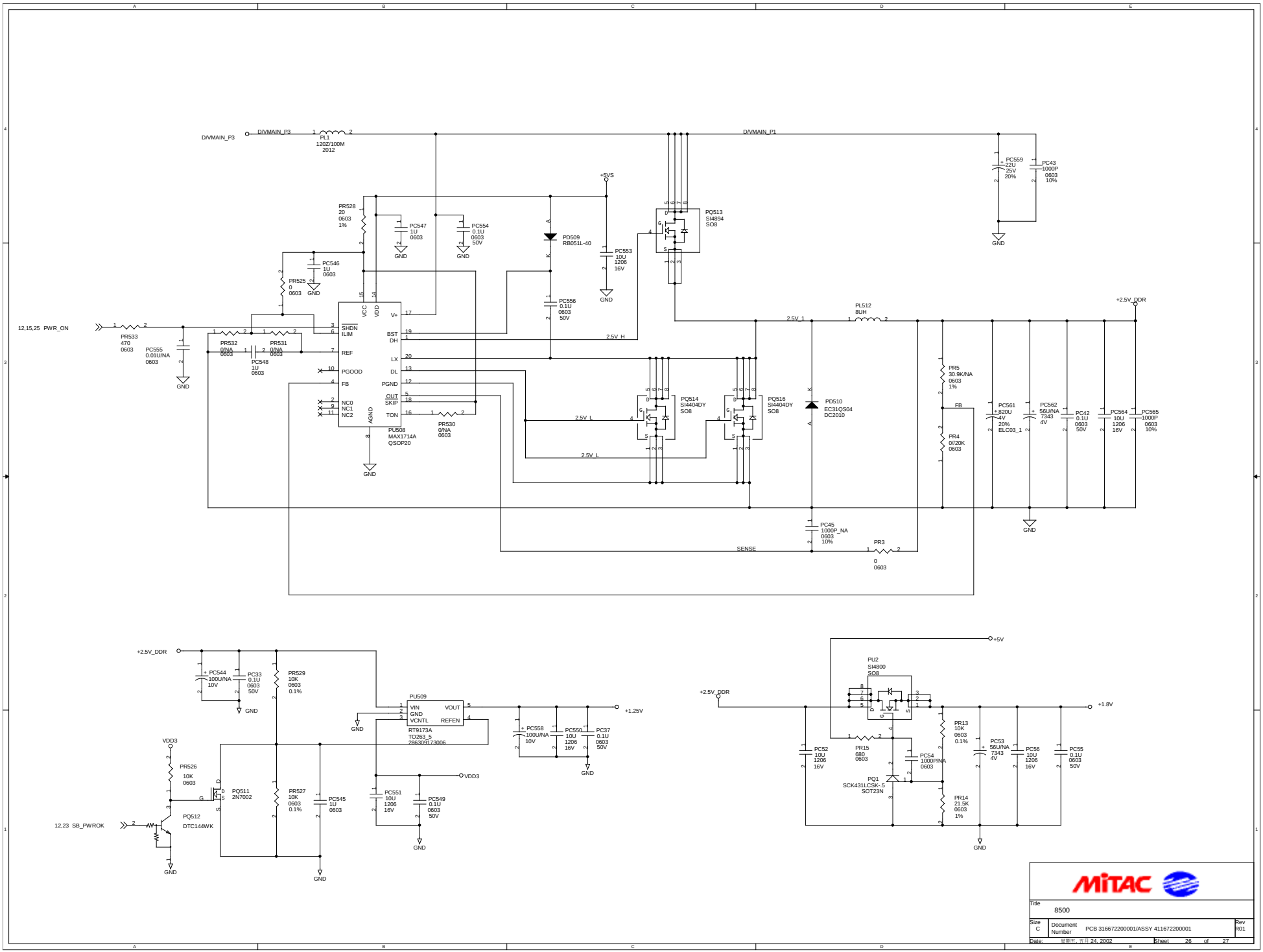

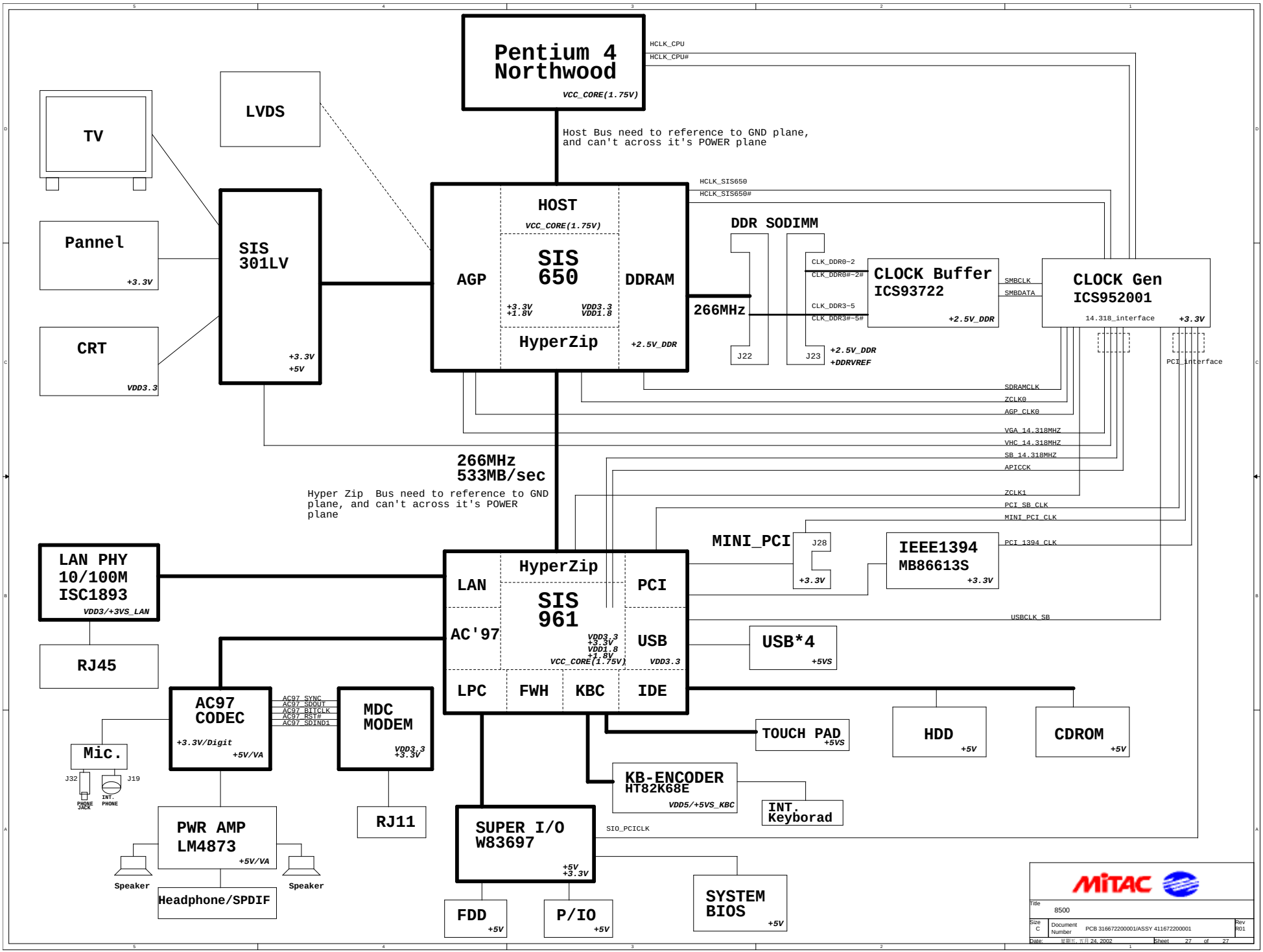

Reference Material

❖ Intel Pentium 4 Processor mPGA478 Socket	Intel, INC
❖ SiS650 IGUI Host / Memory Controller	SiS, INC
❖ SiS691 MuTIOL Media I/O Controller	SiS, INC
❖ SiS301LV / Chrontel CH7017 TV/LVDS Encoder	SiS, INC
❖ W83697HF Super I/O Controller	WinBond, INC
❖ MB86613L IEEE1394 Controller	Fujitsu, INC
❖ 8500 Hardware Engineering Specification	*Technology Corp.*/MiTAC

SERVICE MANUAL FOR 8500

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