


6120 Mother BD		
Page	Description	Comments
1.	Title	
2.	CPU Celeron Socket 370	
3.	North Bridge 443BX	
4.	SO-DIMM	
5.	On Board SDRAM	
6.	Synthesizer	
7.	PIIX4	
8.	IDE & FDD conn	
9.	VGA ATI Rage LTpro	
10.	VGA connector	
11.	SGRAM	
12.	Pci card controller T11225	
13.	Pci card Socket	
14.	PCI Audio CS4280	
15.	AC97 CODEC CS4297	
16.	Audio Amp. TPA202	
17.	Super I/O & RS232	
18.	H8 I/O/KC	
19.	USB & Backlite conn & Port Replicator	
20.	Pull-up & BIOS	
21.	Power Peripheral	
22.	Modem & Battery Charger D/D conn	
REV	Description of Change	Comments
R00	Initial Design	Difference from 6020 1. CPU change to CELERON/PPGA Socket370) 2. Use BX chipset in Desktop mode 3. Add Core/Bus Ratio frequency select circuits 4. Add thermal translation 5. Connect SLP#(from CPU) to PIIX4 for sleep mode (Mobile use quick start mode) Power management 1. w/ AC--> POS(Ring wake up support) PIIX4 SUSM# active HB STR# SUSBNS# always high 2. w/o AC--> STR(No Ring wake up support) System command to HB STR# active System prepare STR procedure(frame buffer content, caribus content...), and after at least 500us PIIX4 SUSM# SUSBNS# active HB SUSBNS# active ROA DVT Change from R00 to ROA 1. Only POS implemented, delete STR function 2. Connect GPO1 to CS4280 as PCIRST# 3. Fix LCDVCC supply circuit 4. Change SGRAM from 4MB to 8MB (total) 5. Change LCD connector from one(20pins) to two parts(2 pins & 30 pins) 6. Add EMI required parts ROB EMI TEST ROD EMI TEST ROE EMI TEST ROF EMI TEST-----PVT RO1 Change from ROF (8-layer) 1. Move via away from port replicator 2. Move Q18 and L25 away from drill hole 3. Q23 reverse 4. R177 change from 10K to 4.7K 5. On component side, the solder mask of CPU socket pin cover 50% of pad ring to get better soldering 6. The damping of SGRAM data bus change to DFS 7. Add LDO regulator to supply +5V to modem (to reduce modem noise)
6120L	modified from 6120R01	
R00	factory request	Modify 1. CPU socket solder side solder mask cover 50% ring pad 2. modify PIO connector (bigger fix hole) 3. modify port replicator connector (pin shift right) 4. modify board edge(add one connection and cut HDD connector part) costdown 1. change diode BAT54 to RL5414B(D3,13,21) 2. BX->ZX(add RP85,86,R244,245) 3. SDRAM data switch change from U17 to Q40,41,42,R239,240,241 4. remove SDRAM US-8,R26,27,C36,37,38-39,80-85 5. R166 10K->2.7K,R167 33->330 6. C115-118 10U->1U 7. remove U36,C307-309,RP85 8. C16,310 10U->100U 9. add R242,243,F3,F4 10. add SAMSUNG SGRAM
6120R	modified from 6120LR00	
R00		Modify 1. Support PIII FC-PGA CPU 2. Change HBF3434 to HS 87570 3. Add track point

DRAWN	DESIGN	CHECK	ISSUES	 MITAC INTERNATIONAL CORP.	
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